PATENT APPLICATION
Attorney Docket No. 1482-0132
Client Ref. No. APD1221-2-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Barrie Gilbert
Serial No.:	09/545,691
Examiner:	Philip Sobutka
Filed:	April 7, 2000
Group Art Unit:	2618
For:	RF MIXER WITH INDUCTIVE DEGENERATION
Date:	August 5, 2009

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SECOND SUBSTITUTE APPEAL BRIEF

This Appeal Brief is in response to the Notification of Non-Compliant Appeal Brief mailed in this case on October 13, 2006. Appeal is taken from the Examiner's Final Office Action mailed June 4, 2004 finally rejecting claim 15.

REAL PARTY IN INTEREST

The present application has been assigned to the following party:

Analog Devices, Inc.
One Technology Way
Norwood, MA 02062

RELATED APPEALS AND INTERFERENCES

The Board's decision in the present Appeal will not directly affect, or be directly affected, or have any bearing on any other appeals or interferences known to the appellant, or to the Applicant's legal representative.

STATUS OF CLAIMS

Claims pending in the application: 2-3, 9-10, 13 and 15-26

Claims 1, 4-8, 11-12 and 14 are cancelled.

Claims drawn to allowable subject matter: 2-3, 9-10, 13 and 16-26

Claims rejected: 15 (which is finally rejected)

Claims appealed: 15

STATUS OF AMENDMENTS

No amendments have been filed subsequent to final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 15 recites an amplifier cell having two input terminals and two output terminals. The cell includes two class AB input stages, each of which drives both of the output terminals in response to an input signal received at one of the input terminals. An example embodiment of such an amplifier is shown in Fig. 26. In the circuit of Fig. 26, transistors Q1, Q2 and Q3 form a first class AB input stage that drives the output terminals 38 and 40 in response to a first input signal V_{IN1}. Transistors Q4, Q5 and Q6 form a second class AB input stage that drives the output terminals 38 and 40 in response to a second input signal V_{IN2}. See page 20, lines 24-29.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claim 15 is unpatentable under 35 U.S.C. 103(a) based on U.S. Patent No. 5,789,799 to Voinigescu et al. ("Voinigescu") in view of U.S. Patent No. 5,307,512 to Mitzlaff ("Mitzlaff").

ARGUMENT

The present patent application discloses amplifiers having, among other things, several types of input stages that drive two output terminals responsive to a single input signal. An example embodiment of such an input stage is shown as item 26 in Fig. 3 where transistors Q11, Q12 and Q13 form a class AB input stage that drives output terminals 38 and 40 in response to a signal received at input terminal 44.

The invention recited in claim 15 takes this concept a step further by combining two class AB input stages to drive the output terminals in response to two input signals, thus providing

fully differential operation. An example embodiment of such an amplifier is shown in Fig. 26. In the circuit of Fig. 26, transistors Q1, Q2 and Q3 form a first class AB input stage that drives the output terminals 38 and 40 in response to a first input signal V_{IN1}. Transistors Q4, Q5 and Q6 form a second class AB input stage that drives the output terminals 38 and 40 in response to a second input signal V_{IN2}.

Claim 15 reads as follows:

15. An amplifier cell comprising:

first and second input terminals;

first and second output terminals;

first class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a first input signal received at the first input terminal; and

a second class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a second input signal received at the second input terminal.

Thus, claim 15 recites two input stages of a specific type that are arranged in a well-defined manner.

In the Office Action (paper No. 20) mailed December 12, 2003, the examiner rejected claim 15 and identified specific circuit elements in the Voinigescu reference alleged to satisfy elements recited in claim 15. However, the Examiner's arguments with respect to the prior art are incorrect in terms of (1) what the elements are, and (2) how the elements are arranged.

Claim 15 recites a second class AB input stage. The Examiner alleges that transistors Q3 and Q6 in Fig. 9 of Voinigescu, although not a class AB circuit, still satisfy the requirement of an "input stage." However, the Voinigescu reference does not support this interpretation. Transistors Q3 and Q6 are not an "input stage," but instead are part of a "mixing quad" formed by transistors Q3, Q4, Q5 and Q6. (See col. 14, lines 31-32 of Voinigescu.)

One skilled in the art would not interpret the mixing quad formed by transistors Q3, Q4, Q5 and Q6 (much less the artificial combination of transistors Q3 and Q6 taken alone) as an

"input stage" as recited in claim 15. This is born out by the Voinigescu reference itself, which distinguishes between an input stage (see col. 14, lines 29-30 referring to transistors Q1 and Q2 in Fig. 9 as an "input pair") and a mixing quad (see col. 14, lines 31-32). This is also supported by the entirety of Applicant's specification, which consistently distinguishes between a mixer core and an input stage. (See, e.g., page 5, line 27 of the specification referring to the mixer core 24 and input section 26 of Fig. 3.)

Additional evidence of the conceptual separation of the mixing core and other stages can be found in the article "Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer", *IEEE Journal of Solid-State Circuits* by P.J. Sullivan, B.A. Xavier and W.H. Ku, Vol. 32, No. 7, July 1997, pp. 1151-1155 (the "Sullivan article"). For example, the Sullivan article refers to an "amplifier section" (page 1151, second column, third line from bottom) (note that claim 15 is drawn to an "amplifier cell") and a "mixer core" (page 1152, second column, second line from bottom).

Thus, Voinigescu does not disclose a second input stage as recited in claim 15.

Claim 15 also recites a first class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a first input signal. The examiner alleges that transistors Q1 and Q2 in Fig. 9 of Voinigescu satisfy this limitation. Applicant concedes that transistors Q1 and Q2 form an input stage. However, it is not a class AB input stage, and it is not arranged as recited in claim 15 if one accepts the Examiner's interpretation of Voinigescu's IF- and IF+ terminals as being the first and second output terminals.

The Examiner acknowledges that Voinigescu does not disclose class AB input stages, but alleges that Mitzlaff provides the motivation to modify Voinigescu to use class AB input stages "for higher efficiency when in FM operation". As discussed above, Voinigescu does not teach two input stages arranged as recited in claim 15, and therefore, cannot serve as a basis for modification according to the teachings of Mitzlaff. Nonetheless, assuming for the sake of argument that the Examiner's analysis of Voinigescu is correct, Mitzlaff does not teach the desirability of using any particular type of input stage. Rather, Mitzlaff simply discloses the benefit *of driving an input stage into saturation* regardless of whether the input stage is class A, class AB, etc. (Col. 2, line 62-66.) Thus, Mitzlaff does not provide any suggestion or motivation to combine the references, and a *prima facie* case of obviousness has not been established.

In the Final Office Action (Paper No. 23) mailed June 4, 2004, the Examiner summarily dismissed Applicant's arguments and stated that they are not relevant because claim 15 does not recite a mixer core. As best understood by applicant, the Examiner seems to be arguing that, since claim 15 does not recite a mixer core, there is no need to distinguish between input stages and mixer cores in the prior art. But such a position is inconsistent with the axiom that claims are presumed to have the meaning attributed to them by those of ordinary skill in the art. As established above, input stages and mixer cores are understood to be different things to those of ordinary skill in the art. To interpret components of a mixer core as an input stage is an unreasonable interpretation. Moreover, the Examiner's tersely worded statement fails to explain how the interrelation of components recited in claim 15 would be satisfied under the Examiner's interpretation of claim terms.

CONCLUSION

Applicant requests that the rejection of claim 15 be reversed.

Respectfully submitted,

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CLAIMS APPENDIX

The claim involved in the appeal reads as follows:

15. (Rejected) An amplifier cell comprising:

first and second input terminals;

first and second output terminals;

first class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a first input signal received at the first input terminal; and

a second class AB input stage coupled to the first and second output terminals and arranged to drive the first and second output terminals responsive to a second input signal received at the second input terminal.

EVIDENCE APPENDIX

Copies of the following references are attached:

U.S. Patent No. 5,789,799 to Voinigescu et al. ("Voinigescu") entered in the record through form PTO-892 as part of Paper No. 6, mailed March 28, 2001.

U.S. Patent No. 5,307,512 to Mitzlaff ("Mitzlaff") entered in the record through form PTO-892 as part of Paper No. 6, mailed March 28, 2001.

"Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer", *IEEE Journal of Solid-State Circuits* by P.J. Sullivan, B.A. Xavier and W.H. Ku, Vol. 32, No. 7, July 1997, pp. 1151-1155 (the "Sullivan article") entered in the record through IDS and form 1449 filed March 11, 2004.

RELATED PROCEEDINGS APPENDIX

None.

US005789799A

United States Patent [19]

Voinigescu et al.

[11] Patent Number: 5,789,799

[45] Date of Patent: Aug. 4, 1998

[54] **HIGH FREQUENCY NOISE AND IMPEDANCE MATCHED INTEGRATED CIRCUITS**

[75] Inventors: **Sorin P. Voinigescu**, Kanata; **Michael C. Maliepaard**, Stittsville, both of Canada

[73] Assignee: **Northern Telecom Limited**, Montreal, Canada

[21] Appl. No.: **727,367**

[22] Filed: **Sep. 27, 1996**

[51] **Int. Cl.**^{6} **H01L 27/082**

[52] **U.S. Cl.** **257/578**; 257/565; 257/567; 257/568; 257/569; 257/570

[58] **Field of Search** 257/578, 531, 257/565, 566, 567, 568, 569, 570, 904; 455/236.1; 363/16, 37, 22, 24

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,928,314	5/1990	Grandfield et al.	455/236
4,980,810	12/1990	McClanahan et al.	363/16
5,164,682	11/1992	Taralp	330/292

OTHER PUBLICATIONS

K.K. Ko et al, "A comparative study on the various monolithic low noise amplifier circuit topologies for RF and microwave Applications" IEEE J. Solid State Circuits vol. 31, No. 8, Aug. 1996, pp. 1220–1225.

F. McGrath et al, in "A 1.9GHz GaAs Chip set for the personal handyphone system", IEEE Trans. MTT vol 43, pp. 1733–1744.

A. Brunel, et al, in "A Downconverter for use in a dual mode AMPS/CDMA chip set", in Microwave J., pp. 20–42, Feb. 1996.

S. Voinigescu, et al "A scaleable high frequency noise model for bipolar transistors with application to optimal transistor sizing for Low noise amplifier design" to be published at the Bipolar Circuits and Technology Meeting, 30 Sep. 1996.

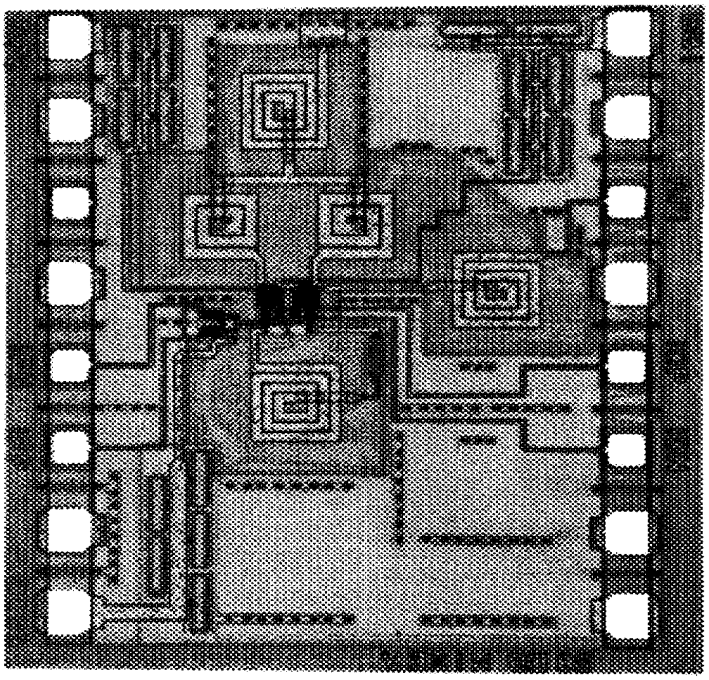
Primary Examiner—Carl W. Whitehead, Jr.

Attorney, Agent, or Firm—Angela C. de Wilton

[57] **ABSTRACT**

An monolithic integrated circuit comprising a transistor-inductor structure is provided having simultaneously noise matched and input impedance matched characteristics at a desired frequency. The transistor-inductor structure comprises a first transistor Q_1 which may be a common emitter bipolar transistor or common source MOSFET transistor Q_1, a second optional transistor Q_2, a first inductor L_E in the emitter (source) of Q_1, and a second inductor L_B in the base (gate) of Q1. The emitter length l_{E1}, or correspondingly the gate width w_g, of Q1 is designed such that the real part of its optimum noise impedance is equal to the characteristic impedance of the system, Z_O, which is typically 50Ω. The first inductor L_E, provides matching of the real part of the input impedance and the second inductor L_B cancels out the noise reactance and input impedance reactance of the structure. The resulting simultaneously noise and impedance matched integrated circuit provides optimal performance. The optimized transistor-inductor structure has particular application to silicon integrated circuits, such as low noise amplifiers and mixer circuits, for wireless and RF circuit applications at 5.8 Ghz, previously reported only for GaAs based circuits. Other basic silicon integrated circuits were optimized at frequencies up to ~12 GHz.

29 Claims, 11 Drawing Sheets



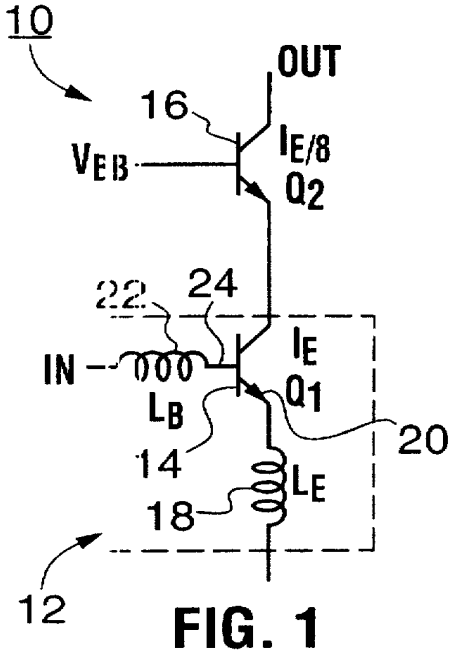


FIG. 1

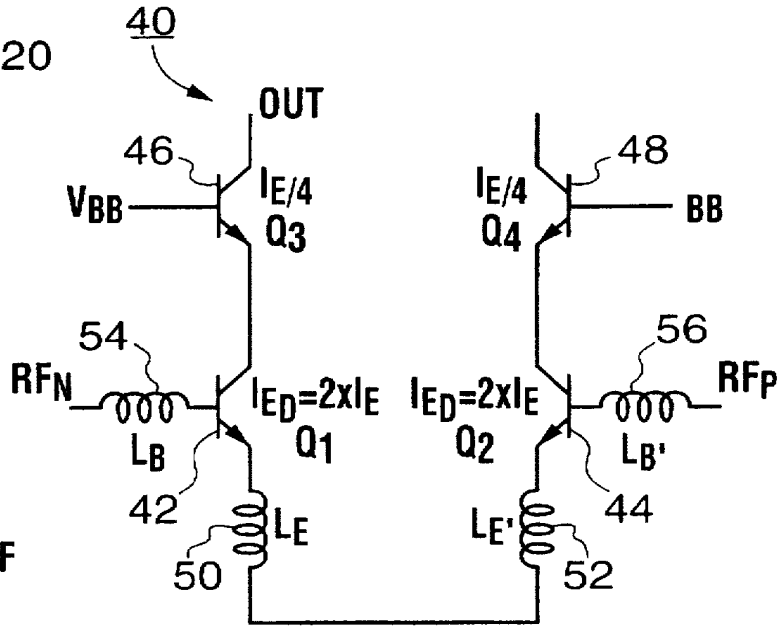


FIG. 2

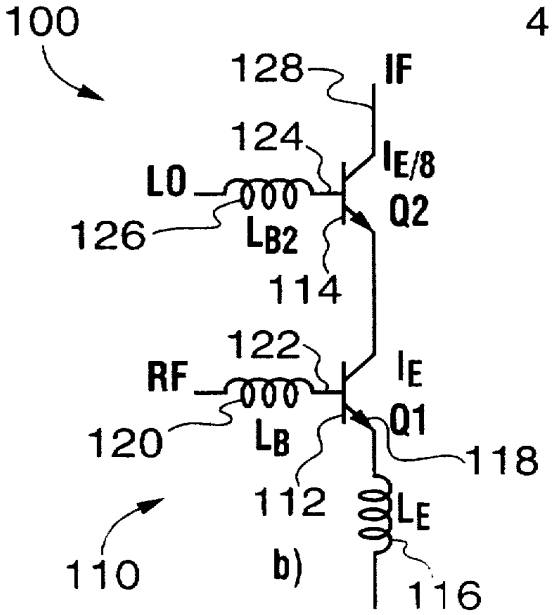


FIG. 3

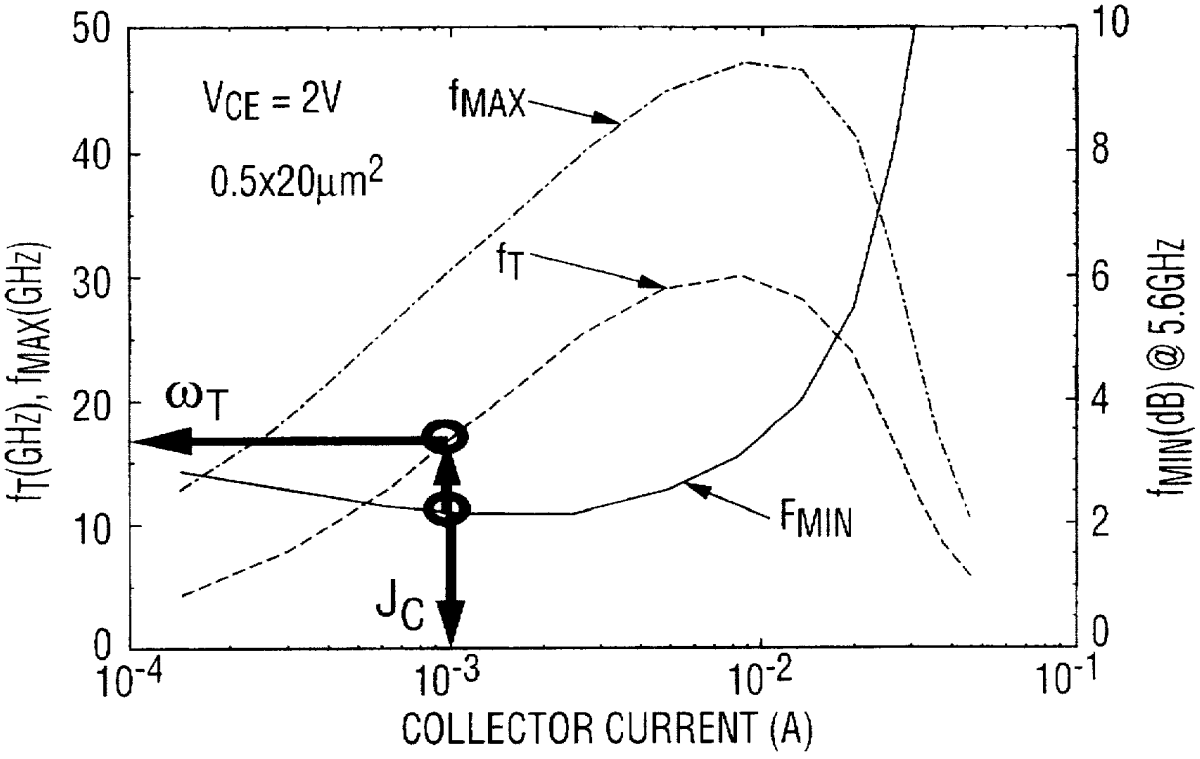

50
40
30
20
10
0
10
8
6
4
2
0
V_{CE} = 2V
0.5x20μm²
f_{MAX}
f_T
ω_T
J_C
F_{MIN}
10^{-4}
10^{-3}
10^{-2}
10^{-1}
COLLECTOR CURRENT (A)
f_T(GHz), f_{MAX}(GHz)
f_{MIN}(dB) @ 5.6GHz

FIG. 4

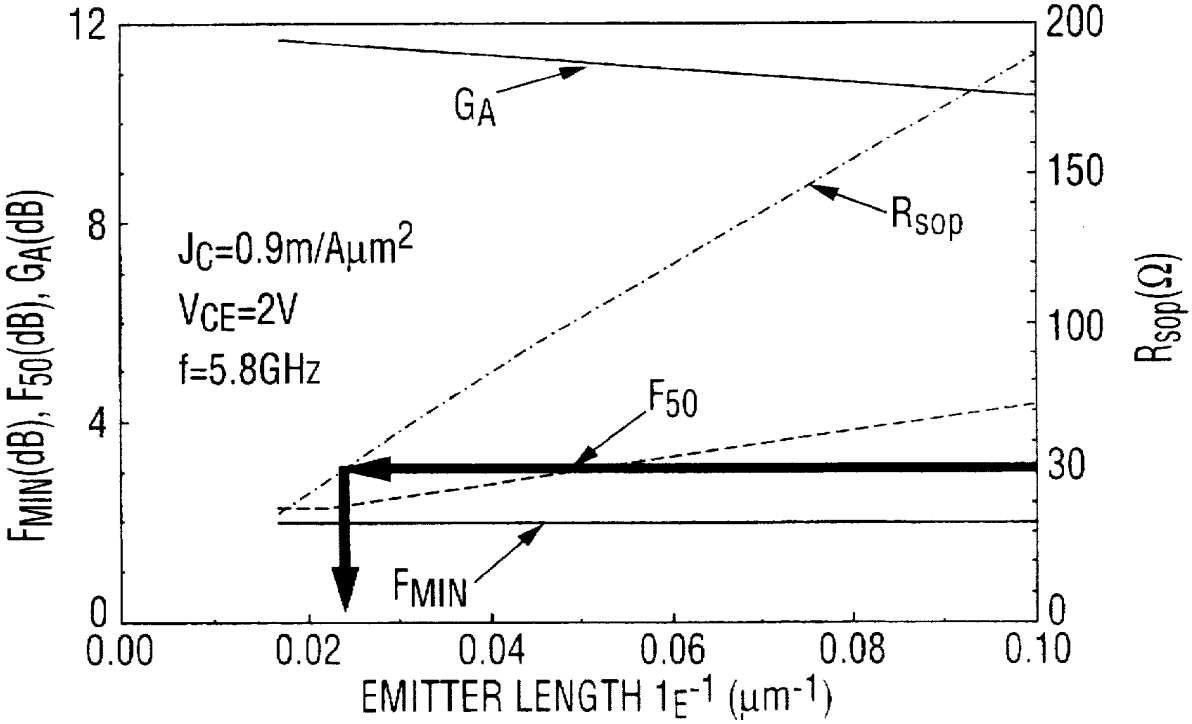

12
8
4
0
200
150
100
30
0
G_A
R_{sop}
F_{50}
F_{MIN}
J_C=0.9m/Aμm²
V_{CE}=2V
f=5.8GHz
0.00
0.02
0.04
0.06
0.08
0.10
EMITTER LENGTH 1_E^{-1} (μm⁻¹)
F_{MIN}(dB), F_{50}(dB), G_A(dB)
R_{sop}(Ω)

FIG. 5

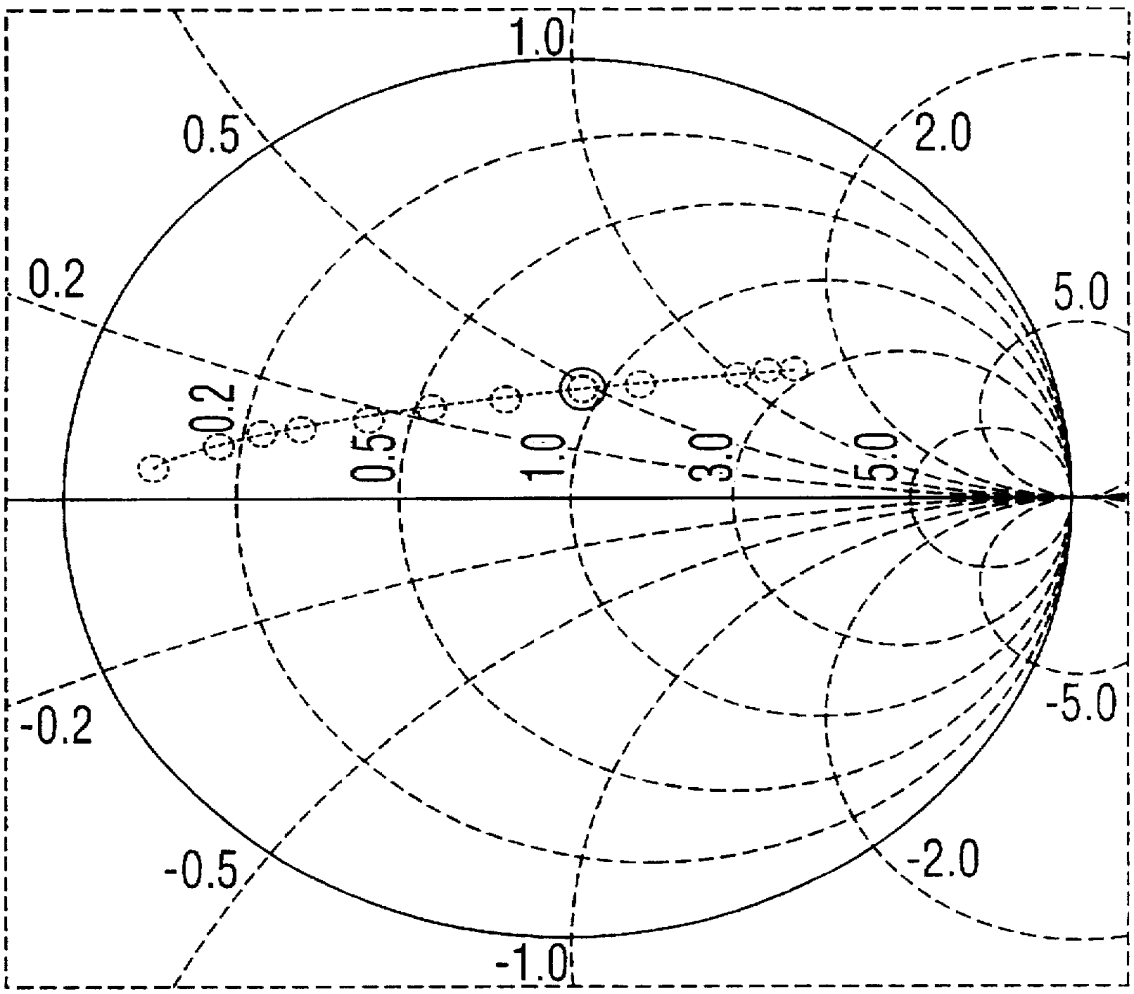

1.0
0.5
2.0
0.2
5.0
0.2
0.5
1.0
3.0
5.0
-0.2
-5.0
-0.5
-2.0
-1.0
Zr: 9.27E-01 Z1: 4.86E-01 SWR: 1.66E+00

FIG. 6

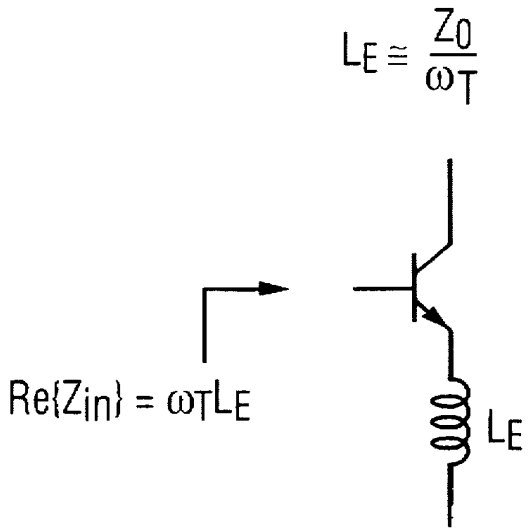

$L_E \cong \frac{Z_0}{\omega_T}$
$Re\{Z_{in}\} = \omega_T L_E$
L_E
Ideal inductor only affects X_{sop}, but not R_{sop}

FIG. 7

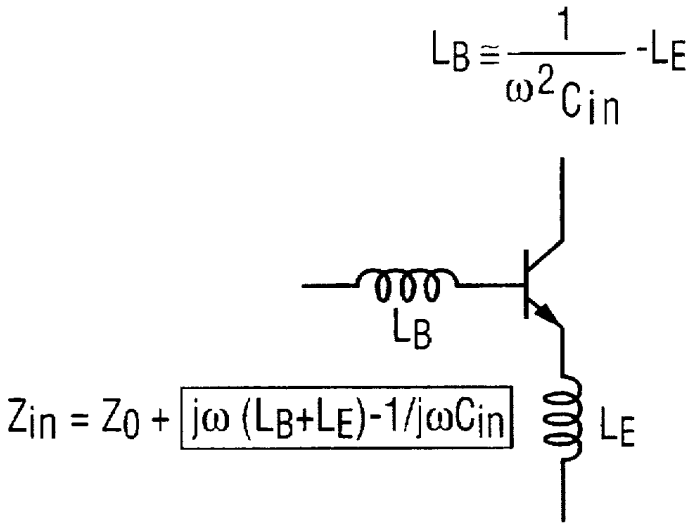

$L_B \cong \frac{1}{\omega^2 C_{in}} - L_E$
L_B
$Z_{in} = Z_0 + \boxed{j\omega (L_B+L_E)-1/j\omega C_{in}}$
L_E

FIG. 8

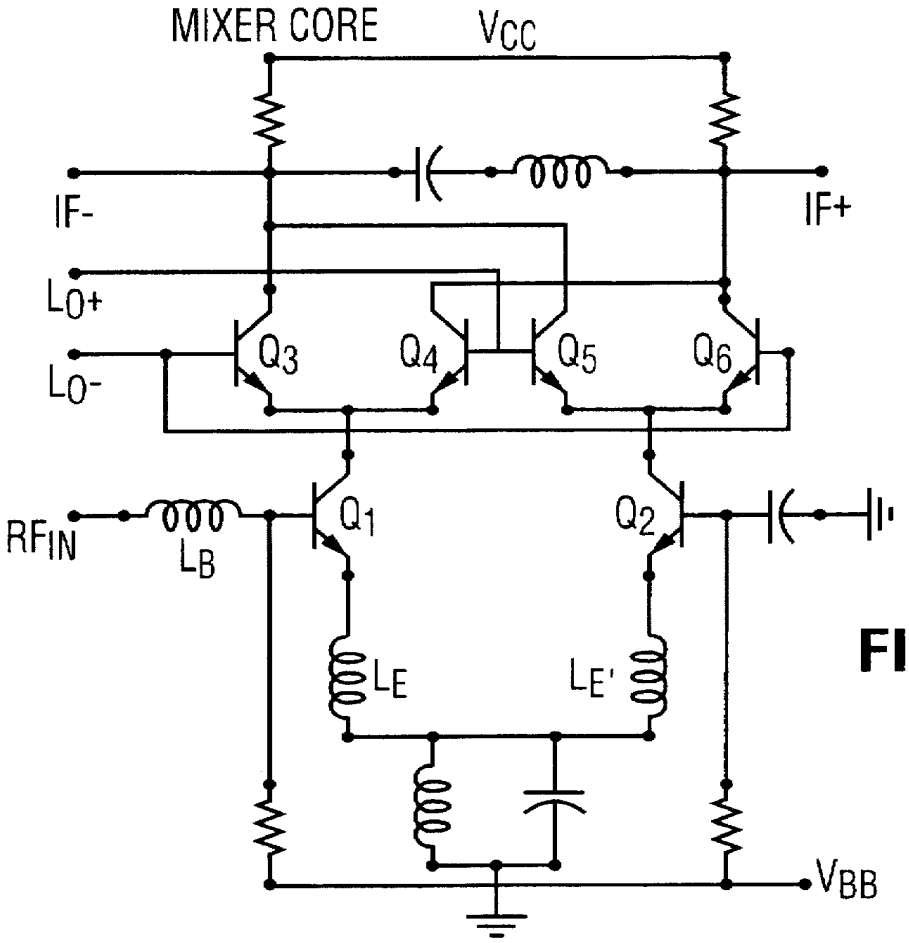

MIXER CORE
VCC
IF-
IF+
LO+
LO-
Q3
Q4
Q5
Q6
RFIN
LB
Q1
Q2
LE
LE'
VBB

FIG. 9

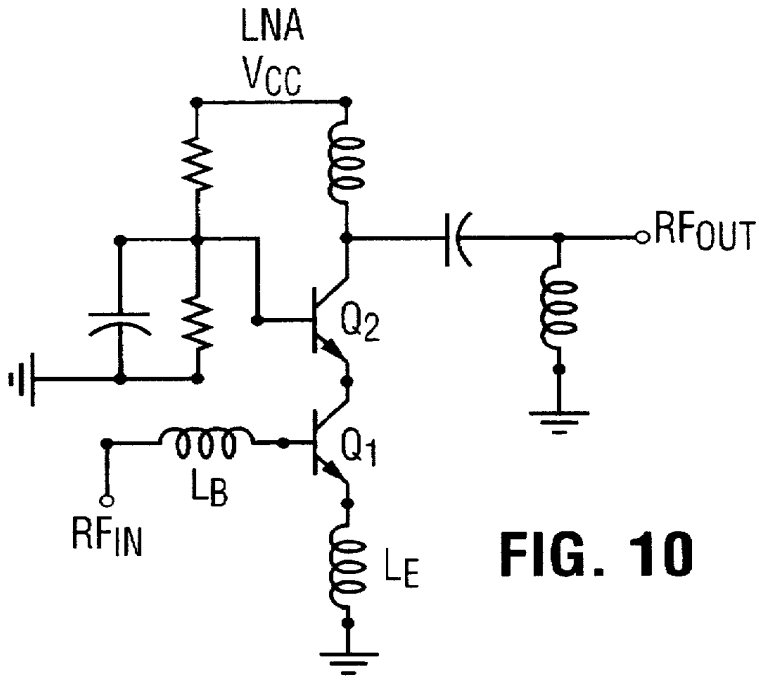

LNA
VCC
RFOUT
Q2
Q1
LB
RFIN
LE

FIG. 10

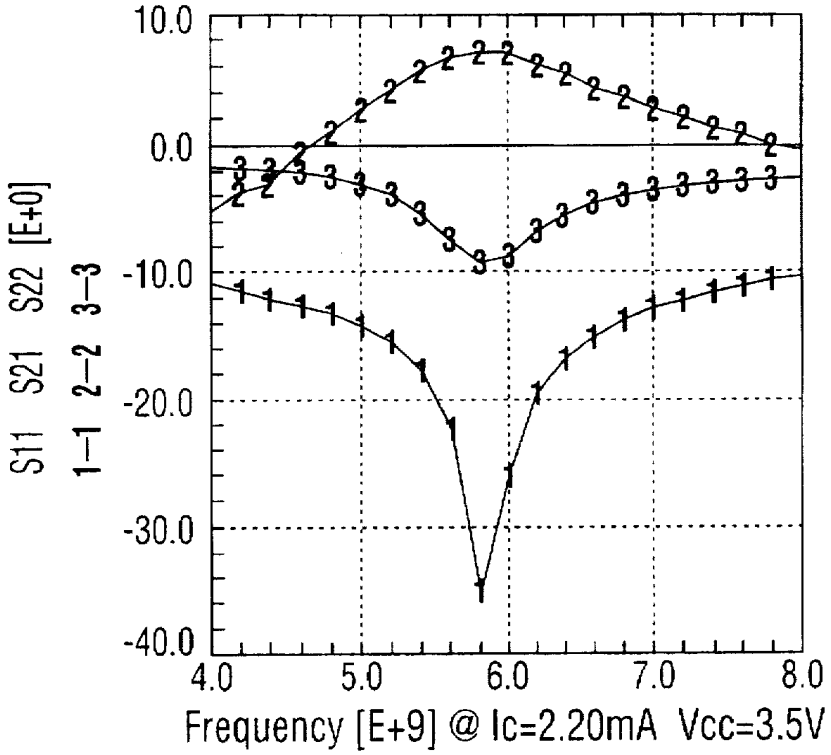

10.0
0.0
-10.0
-20.0
-30.0
-40.0
4.0
5.0
6.0
7.0
8.0
S11 S21 S22 [E+0]
1-1 2-2 3-3
Frequency [E+9] @ Ic=2.20mA Vcc=3.5V

FIG. 11

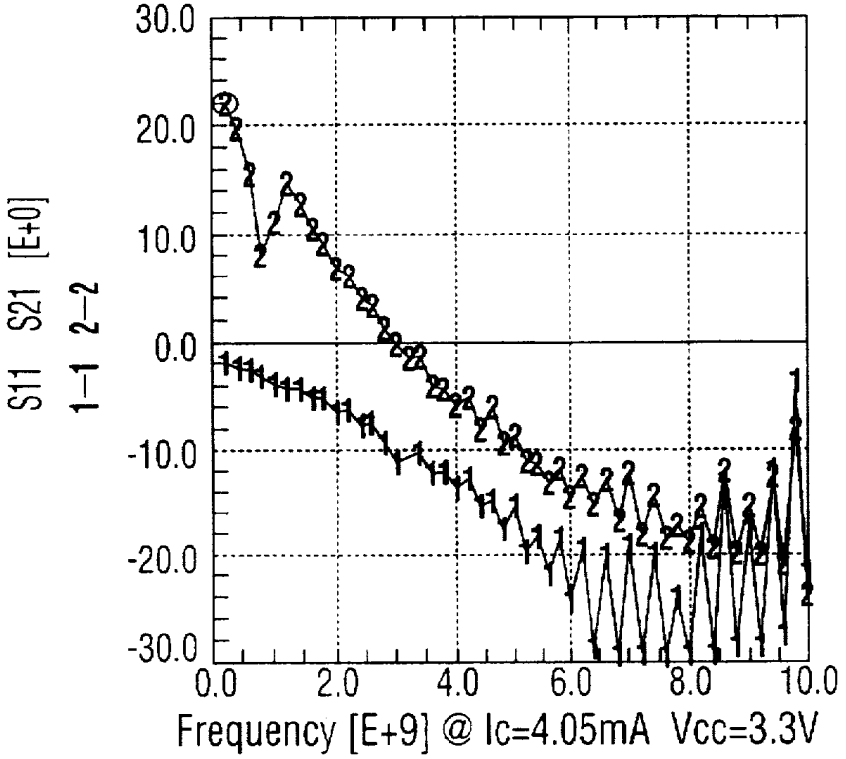

30.0
20.0
10.0
0.0
-10.0
-20.0
-30.0
0.0
2.0
4.0
6.0
8.0
10.0
S11 S21 [E+0]
1-1 2-2
Frequency [E+9] @ Ic=4.05mA Vcc=3.3V

FIG. 12

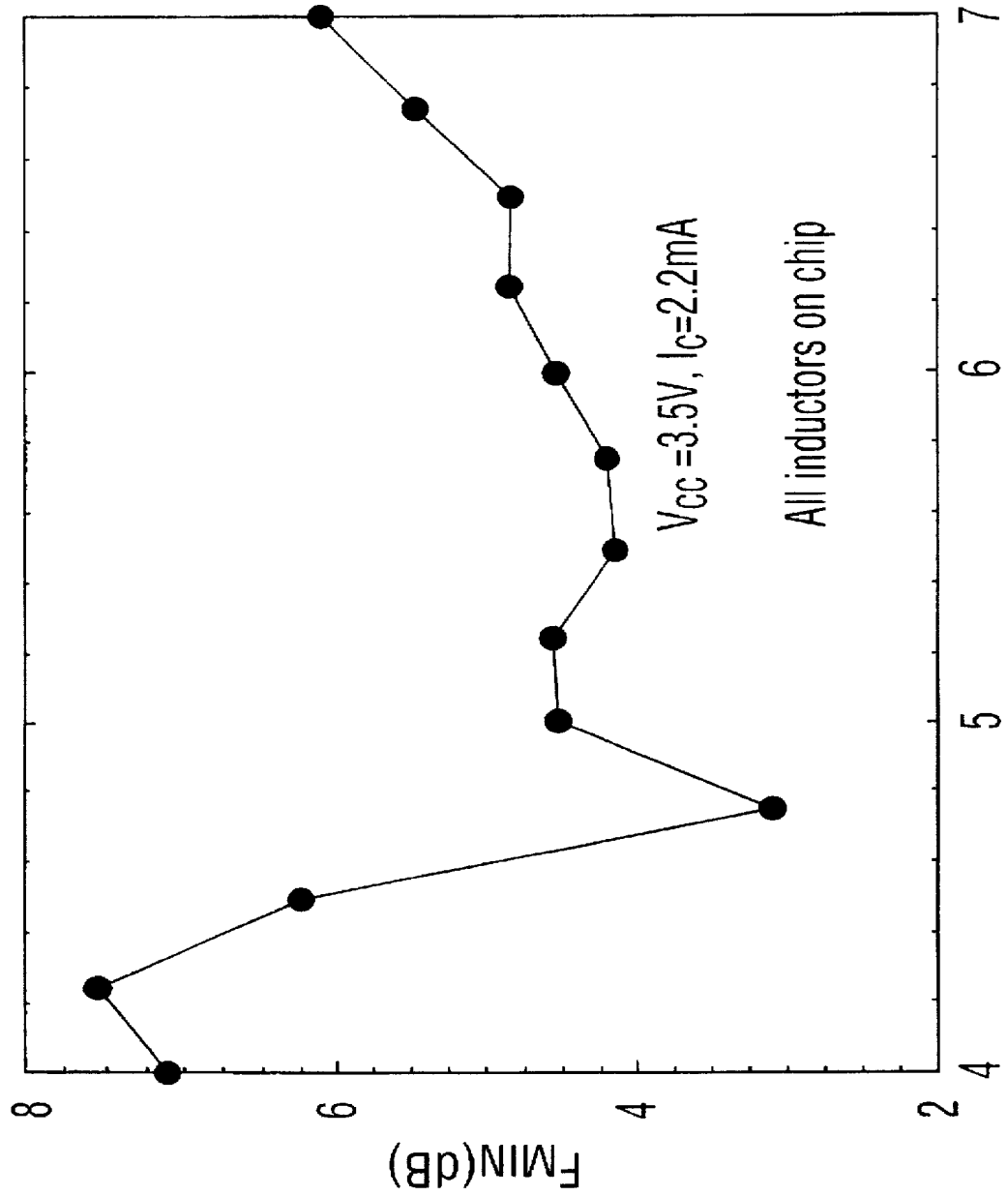

F_{MIN}(dB)
8
6
4
2
4
5
6
7
FREQUENCY (GHz)
V_{CC} =3.5V, I_C=2.2mA
All inductors on chip

FIG. 13

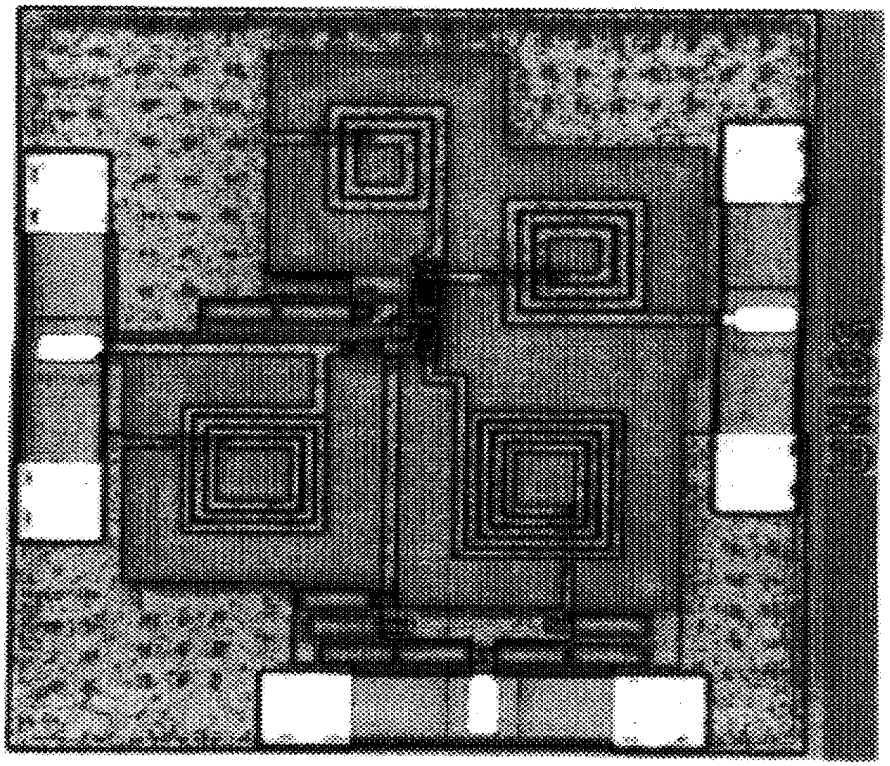


FIG. 14A

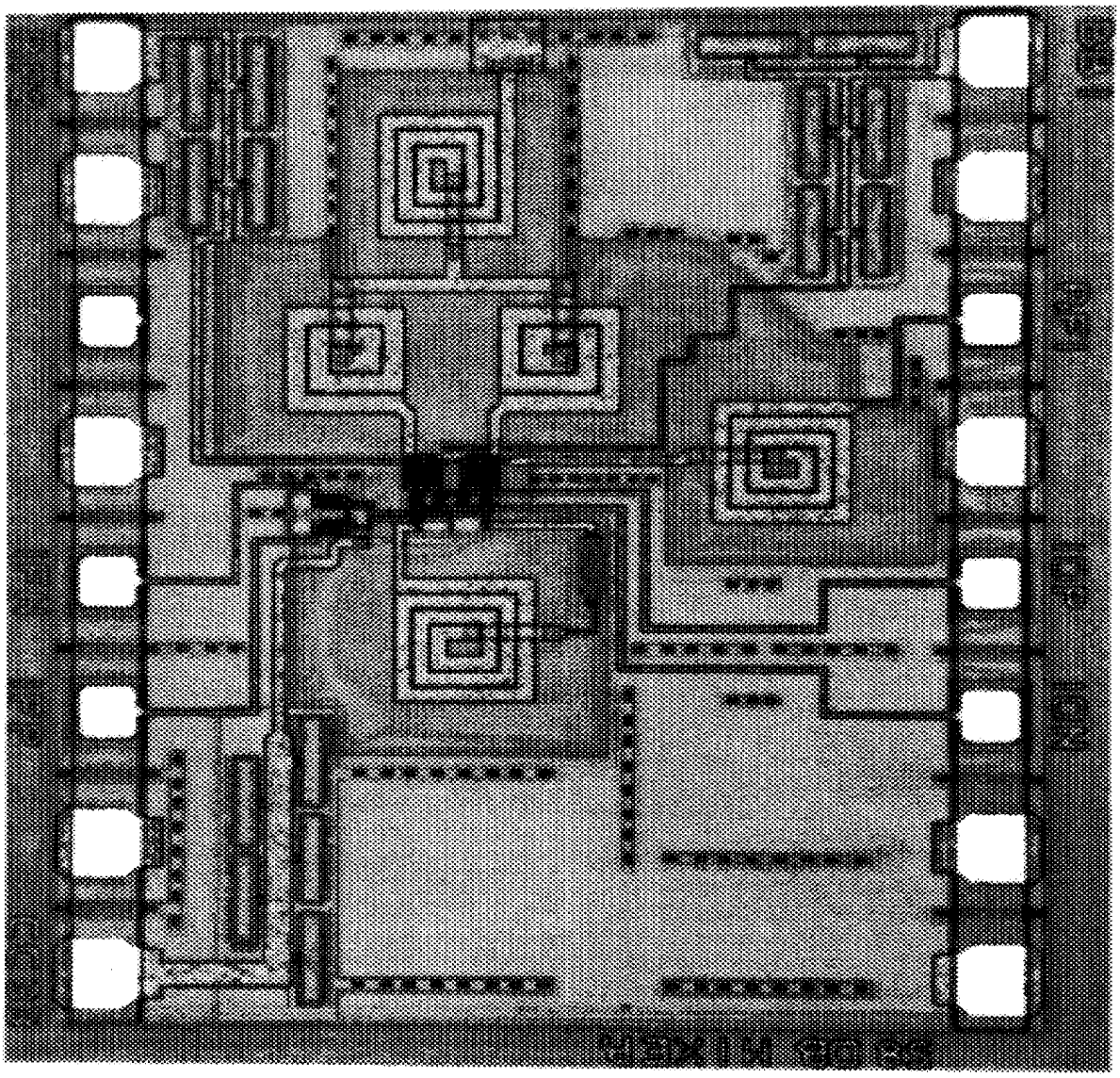


FIG. 15A

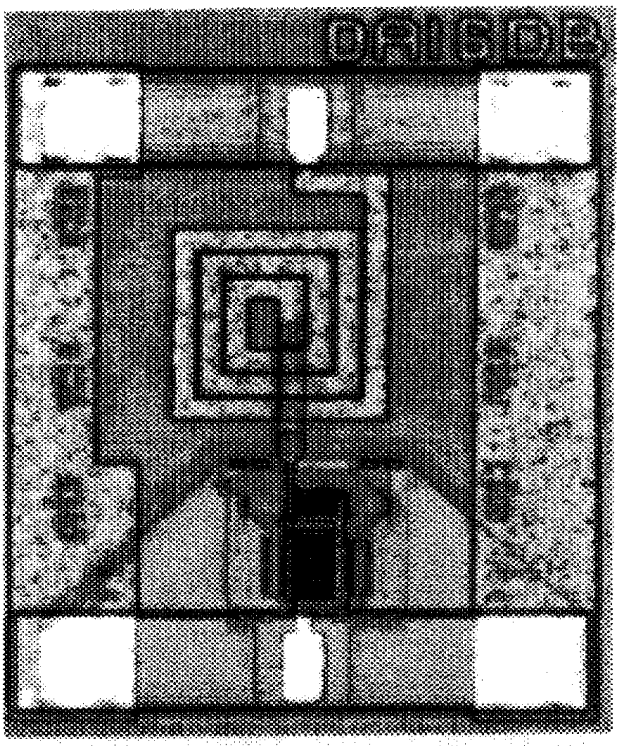


FIG. 16A

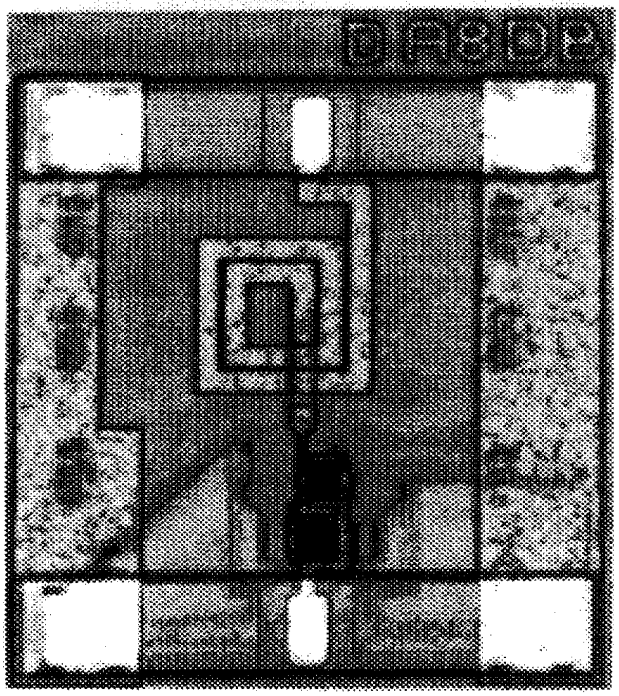


FIG. 17A

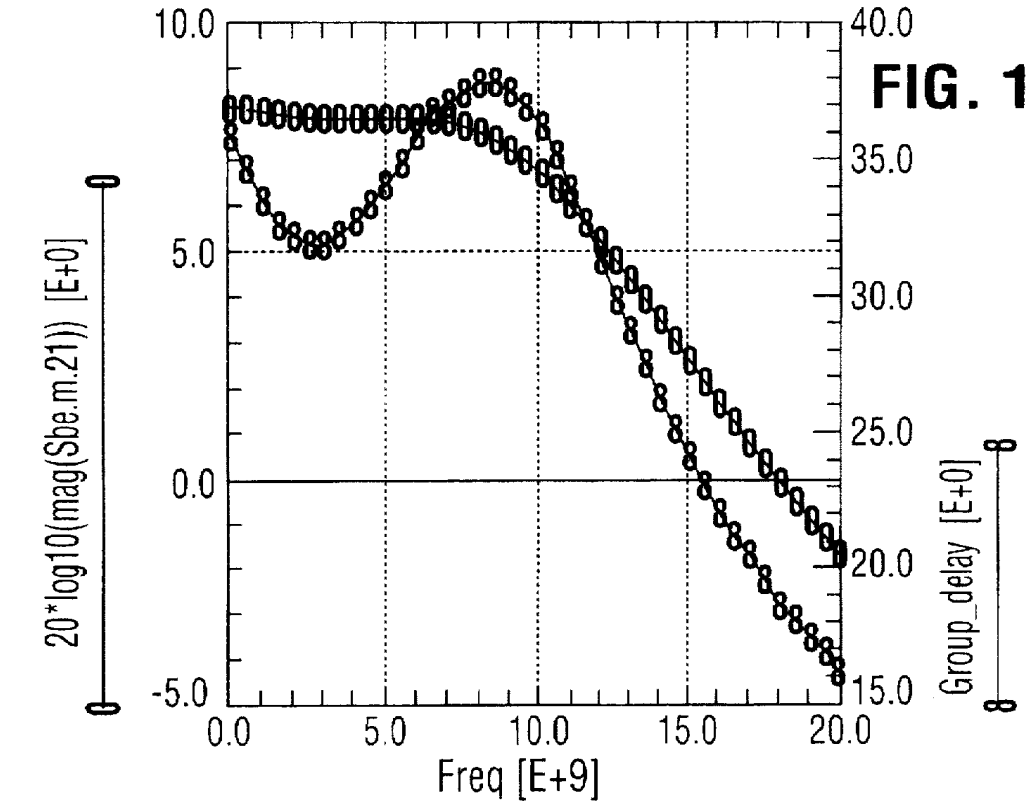

10.0
5.0
0.0
-5.0
40.0
35.0
30.0
25.0
20.0
15.0
0.0
5.0
10.0
15.0
20.0
Freq [E+9]
20*log10(mag(Sbe.m.21)) [E+0]
Group_delay [E+0]

FIG. 18

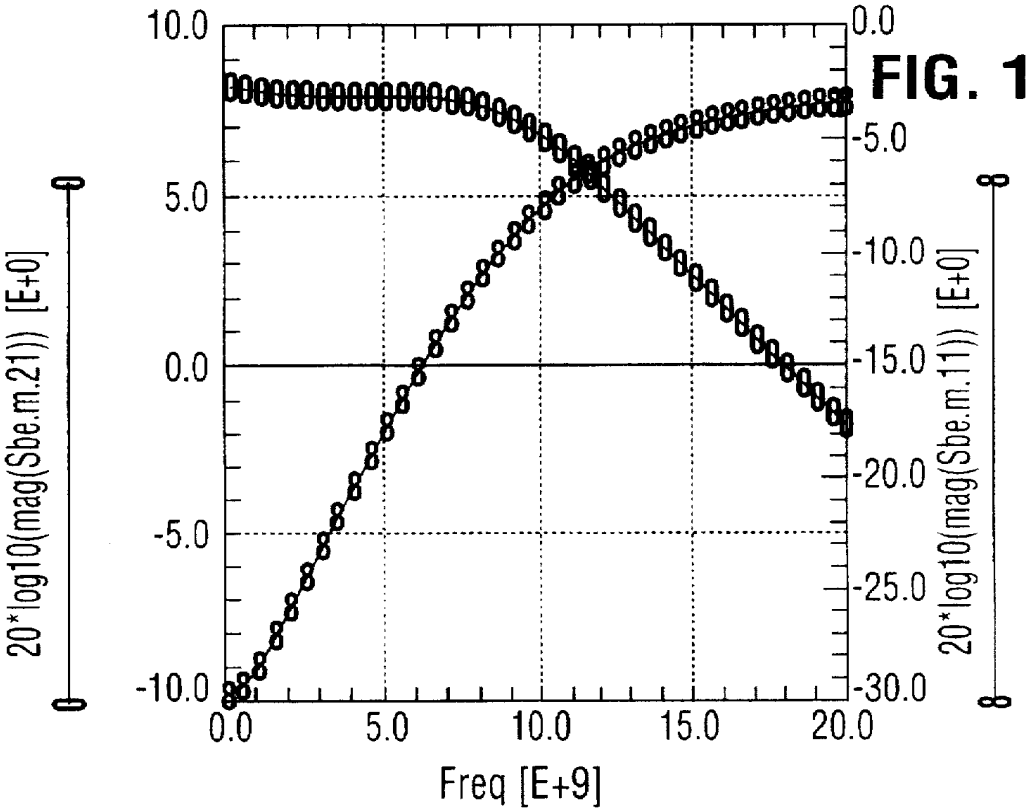

10.0
5.0
0.0
-5.0
-10.0
0.0
-5.0
-10.0
-15.0
-20.0
-25.0
-30.0
0.0
5.0
10.0
15.0
20.0
Freq [E+9]
20*log10(mag(Sbe.m.21)) [E+0]
20*log10(mag(Sbe.m.11)) [E+0]

FIG. 19

HIGH FREQUENCY NOISE AND IMPEDANCE MATCHED INTEGRATED CIRCUITS

FIELD OF THE INVENTION

This invention relates to high frequency noise and impedance matched integrated circuits and a methodology for circuit design, with particular application to silicon integrated circuits using integrated inductors for RF circuit applications.

BACKGROUND OF THE INVENTION

Successful exploitation of wireless consumer products relies on highly integrated, low cost integrated circuits. Steady improvements in transistor performance and demand for higher levels of integration have led to the increased application of silicon technology for RF and wireless circuit applications. Indeed, cost effective silicon-based integrated circuits are now available for wireless personal communications systems at lower bit rates in the ~1 GHz band.

Recent developments in broadband multimedia communications systems are based on wireless asynchronous transfer mode (ATM) transmission in the 5 GHz band. Although GaAs circuits remain several times more expensive than silicon circuits, the feasibility of using lower cost silicon based technology in this frequency band has been limited, due to significantly higher substrate and interconnect losses in silicon relative to GaAs. Historically, silicon technology has suffered from a lack of high Q inductors. More recently, improved inductor performance has been obtained using microstrip transmission line inductors.

Nevertheless, whether designing high frequency GaAs or silicon based circuits, for example, tuned low noise amplifier (LNA) and mixer circuits for wireless systems, simultaneous noise and impedance matching presents a challenge to improved performance. There is a trade-off in noise and input impedance matching, as discussed by K. K. Ko et al, "A comparative study on the various monolithic low noise amplifier circuit topologies for RF and microwave Applications" IEEE J. Solid State Circuits vol. 31, no. 8, August 1996, pp. 1220–1225. This trade-off is caused mostly by the fact that the transistor size is traditionally considered as a fixed design parameter, and a library of certain standards sizes are available. Thus, conventionally, a passive network is designed around a given transistor in order to achieve noise matching and/or impedance matching. The passive network itself contributes losses and degrades the noise figure, as discussed by F. McGrath et al, in "A 1.9 GHz GaAs Chip set for the personal handyphone system", IEEE Trans. MTT Vol. 43, pp. 1733–1744, 1995 and by A. Brunel, et al. in "A Downconverter for use in a dual mode AMPS/CDMA chip set", in Microwave J., pp. 20–42, February 1996.

The losses in the passive network increase as the network become more complicated, and a significant area of an integrated circuit may be taken up by the matching network. For example, in typical low noise amplifiers and GaAs mixer circuits discussed in the above mentioned references to Ko, McGrath and Brunel, either the noise figure or input impedance matching are sub-optimal, or the passive matching circuit is excessively complex, occupying a large semiconductor area.

It is well known that high frequency losses are particularly severe on semiconducting silicon substrates, relative to semi-insulating GaAs substrates. On the other hand, while passive components are less lossy on GaAs substrates, the present cost of GaAs circuits is at least a factor of two more

expensive than silicon circuits. Consequently, if matching losses were reduced for silicon substrates to allow for design of high performance wireless circuits, these circuits could be fabricated in silicon with significant cost savings relative to similar GaAs circuits.

SUMMARY OF THE INVENTION

The present invention seeks to provide improved noise and impedance matching for monolithic integrated circuits, particularly for silicon integrated circuits for high frequency applications in RF and wireless technology, and a design methodology for integrated circuits, which overcomes or avoids the above mentioned limitations.

Thus according to one aspect of the present invention there is provided an integrated circuit including an integrated transistor-inductor structure comprising:

a transistor having geometric dimensions comprising a characteristic dimension, the characteristic dimension being an emitter length, l_E for a bipolar transistor, and a gate width w_g for field effect transistor, the characteristic dimension being selected to provide the real part of the optimum noise impedance equal to the characteristic impedance of the integrated circuit Z_O, thereby providing noise matching of the transistor at a selected operating frequency and bias current density;

and a passive matching network consisting of a first inductor for matching the real part of the input impedance to Z_O, and a second inductor for cancelling out the imaginary part of the input impedance and the noise reactance respectively, the circuit thereby providing simultaneous noise and input impedance matching.

Optimization of the transistor geometry achieves noise matching of the transistor and reduces the number of network matching components required to meet impedance and noise specifications of the circuit, and thus significantly reduces the circuit area. The noise and impedance matched integrated circuit structure comprising an optimised integrated-transistor-inductor structure provides improved performance at high frequencies suitable for RF and wireless circuit applications such as telecommunications.

The first inductor is selected to provide matching of the real part of the input impedance and is approximated by $L_E=Z_O/\omega_T$. The second inductor matches the imaginary part of the input impedance and the noise impedance to 0_Ω by setting $L_B=1/\omega^2C_{in}-L_E$.

Typically the characteristic impedance of the system Z_O is 50Ω. Z_O may be increased from the typical 50Ω, if required, in order to improve performance further.

Where the integrated circuit comprises a bipolar transistor comprising an emitter, base and collector, coupled in common emitter configuration, the length l_E of the emitter is optimized to provide noise matching of the transistor, and the first inductor is an emitter coupled inductor L_E for matching the real part of the input impedance Z_O, and the second inductor is a base coupled inductor L_B for matching the imaginary part of the input impedance and noise reactance to 0Ω.

Alternatively, when the transistor comprises a field effect transistor comprising a gate, source and drain, coupled in common source configuration, the width w_G of the gate is optimized to provide noise matching of the transistor, and the first inductor is a source coupled inductor L_E for matching the real part of the input impedance Z_O, and the second inductor is a gate coupled inductor L_B for matching the imaginary part of the input impedance and noise reactance to 0Ω.

Practically, a second transistor Q2 is added for input/output buffering, the second transistor being coupled to the first transistor in cascode configuration, and size ratio of Q1 to Q2 being determined by the ratio of the peak f_T current density and the minimum noise current density.

Thus according to another aspect of the present invention, there is provided an integrated circuit including an integrated transistor-inductor structure comprising:

first and second bipolar transistors in cascode configuration, each transistor comprising an emitter, collector and base, the first transistor being coupled in common emitter mode and the second transistor coupled in common base mode,

the first transistor having a emitter length l_E, selected to provide to provide the real part of the optimum noise impedance equal to the characteristic impedance of the integrated circuit Z_O, thereby providing noise matching of the transistor at a selected operating frequency;

a first inductor L_E coupled to the emitter of the first transistor, for matching the real part of the input impedance to Z_O, and a second inductor L_B, coupled to the base of the first transistor, for cancelling out the imaginary part of the input impedance and the noise reactance respectively, the circuit thereby providing simultaneous noise and input impedance matching.

The emitter length l_{E2} of the second transistor is selected to provide that it is biased at the current density at which its cutoff frequency reaches a maximum for maximizing gain and frequency of operation. The size ratio, i.e. the ratio of the emitter lengths, of the first and second transistors is determined by the ratio of the peak f_T current density to the minimum noise current density.

The design of the transistor-inductor structure is based on a novel approach to design methodology in which the size of the transistor is designed first so that real part of the optimum noise impedance of the transistor is noise matched to the characteristic impedance of the system Z_O, typically 50Ω, at the desired frequency and collector current density. Since the transistor is an active device, noise matching is achieved without losses and without noise figure degradation. The task of noise matching of the transistor is thus removed from the passive network. Losses in the passive network around the transistor are reduced, and the resulting matching network is therefore simpler, and less lossy than in current known circuit designs.

To complete the noise and impedance matched structure, a minimal passive network comprising only two lossless inductors is designed to provide impedance matching with the lowest possible degradation of the overall noise figure. The simplified matching network reduces components and saves area, contributing to significant cost reduction.

The noise and impedance matched transistor-inductor structure may be used to build integrated circuits such as low noise amplifiers and mixer circuits with significantly improved performance at high frequencies. Performance of noise and impedance matched silicon transistor-inductor devices has been obtained which is comparable to that of GaAs at frequencies in the 1 to 12 GHz range.

For example, the noise matched transistor-inductor structure may provide a circuit operable as a low noise amplifier, comprising: means for supplying a first input signal coupled to the first transistor base through the second inductor L_{B2}; the transistor emitter coupled to an emitter degeneration means comprising the first inductor L_E; and output means coupled to the collector of the first transistor for generating an output signal.

Correspondingly, the transistor-inductor structure may be used to provide a circuit operable as a mixer, comprising: means for supplying an first input (RF) signal coupled to the first transistor base through the second inductor L_B; a second base inductor coupled to the base of the second transistor and means for supplying a second input (LO) signal coupled to the second transistor through the second base inductor; the transistor emitter coupled to an emitter degeneration means comprising the first inductor L_E, for generating an output (IF) signal at output means coupled to the collector of the first transistor.

Each transistor may, for example, be a bipolar transistor selected from the group consisting bipolar junction transistors (BJTs) or heterojunction bipolar transistors (HBTs). Alternatively, the transistors may be field effect transistors, i.e. silicon MOSFETs or MESFETs, JFETs, and HEMT transistors. Thus the noise and impedance matched circuits may be implemented, for example, in silicon, silicon germanium, or a III-V compound semiconductor. By providing simultaneous noise and impedance matching, thereby reducing substrate losses, the design methodology provides for particular improvements in the high frequency performance of silicon based circuits.

The simple and compact integrated transistor-inductor structure is used to demonstrate the feasibility of fabricating a cost effective, high performance, high speed silicon integrated circuit, which is simultaneously noise and impedance matched.

According to a further aspect of the present invention there is provided a silicon integrated circuit structure comprising a integrated transistor-inductor structure for operation as a double balanced mixer comprising:

an input pair of common emitter transistors Q1 and Q2, a mixing quad comprising two differential pairs of common base transistors Q3 and Q4, and Q5 and Q6, each transistor of the input pair Q2 and Q2 coupled to the emitter of a respective one of the pairs of mixing quad;

a pair of emitter inductors L_E coupled to the emitters of the input pair Q2 and Q2, the emitter inductors L_E providing emitter degeneration means, and a base inductor L_B coupled to the base of one of first pair of Q2 and Q2, the other base being AC grounded;

input means for supplying differential input (RF) signals coupled to the bases of the input transistor pair through the second inductor L_B,

input means for supplying differential second input (LO) signals coupled to respective bases of each pair of transistors of the mixing quad,

output means coupled to collectors of pairs transistors of the mixing quad for generating a differential output IF signal; and

each of the transistors of the input pair Q2 and Q2 having a emitter length l_E, selected to provide the real part of the optimum noise impedance equal to the characteristic impedance of the integrated circuit Z_O, thereby providing noise matching of the transistors at a selected operating frequency;

the emitter inductors L_E coupled to the emitter of the input transistors, for matching the real part of the input impedance to Z_O, and the second inductor L_B, coupled to the base of one of the input transistor, for cancelling out the imaginary part of the input impedance and the noise reactance respectively, the circuit thereby providing simultaneous noise and input impedance matching.

The size ratio of the transistors in the mixing quad and the input pair is based on ratio of the peak f_T current density and the minimum noise current density.

Advantageously, the circuit includes an LO reject filter comprising an series LC filter coupled between the differ-

ential IF outputs, and a parallel LC resonator tuned on the second RF harmonic as an AC current source coupled in the emitter of the input pair.

According to another aspect of the present invention there is provided a silicon integrated circuit structure comprising a transistor-inductor structure for operation as a low noise differential amplifier, comprising:

an input pair of common emitter transistors Q1 and Q2, and an output pair of common base transistors Q3 and Q4 coupled in cascode configuration; a pair of emitter inductors L_E coupled to respective emitters of the input pair Q1 and Q2, and a pair of base inductors L_B coupled to the respective bases of the input pair of Q1 and Q2,

means for supplying a first input signal pairs coupled to respectively to the bases of the first transistor pair through the second inductors L_B,

for generating a pair of output signals at the collectors of the second transistors Q3 and Q4;

each of the transistors of the input pair Q1 and Q2 having a emitter length l_E, selected to provide the real part of the optimum noise impedance equal to the characteristic impedance of the integrated circuit Z_O, thereby providing noise matching of the transistors at a selected operating frequency;

the emitter inductors L_E coupled to the emitter of the input transistors, for matching the real part of the input impedance to Z_O, and the base inductor L_B, coupled to the base of one of the input transistor, for cancelling out the imaginary part of the input impedance and the noise reactance respectively, the circuit thereby providing simultaneous noise and input impedance matching.

The emitter lengths of the first and second pairs of transistors are characterized by being twice as large as the corresponding emitter lengths in the corresponding single ended circuit.

Thus, the integrated transistor-inductor structure may be used to advantage in providing various input impedance and noise matched low noise amplifier circuit and a mixer circuit of simple and compact design. In particular, the circuits may be implemented in silicon, and provide high frequency performance more generally found only in GaAs circuits. These structures may be fabricated by known silicon process technology, and implemented in either high speed silicon bipolar or silicon MOSFET technologies. Other high speed silicon based devices, for example SiGe bipolar transistors may alternatively be used.

Specifically, monolithic silicon low noise amplifier and a mixer circuits operable at 5.8 GHz are demonstrated to be feasible with performance characteristics previously reported only for GaAs based circuits. This improved performance at a record high frequency for a silicon based circuit is dependent on several factors. Firstly, the unconventional design methodology presented herein, in which the transistor emitter length is treated as a design variable. Initially, the transistor emitter length is optimised to obtain noise matching, which then allows a very much simplified matching network. Secondly, the use of a high performance silicon bipolar technology takes advantage of recent improvements in inductors and microstrip transmission lines using multilevel metallization schemes. The latter benefit from use of first level metal as ground planes to reduce substrate losses.

Consequently, substrate losses can be reduced, and very significant improvements in performance of silicon based integrated circuits relative to conventional designs can be achieved for high frequency RF circuit applications.

Since the substrate losses in GaAs and other compound semiconductor implementations are lower than in silicon, more modest performance improvements are obtained. Nevertheless, the structure is also beneficial in avoiding the trade-off in noise and input impedance matching in designing GaAs and other III-V compound semiconductors to obtain optimal performance. Accordingly, another aspect of the present invention provides a method for providing a noise and impedance matched integrated circuit comprising an integrated transistor-inductor structure, comprising:

first, determining geometric dimensions of the transistor to provide the real part of the noise impedance of the transistor is equal to the characteristic impedance Z_O at a desired frequency and collector current density;

and then, designing a minimal passive matching circuit comprising a first inductor to provide matching of the real part of the input impedance, and a second inductor cancelling out the noise reactance and input impedance reactance of the structure.

The design is achieved in two stages, I) the noise matched transistor design stage, which optimises noise matching at a selected frequency, and II) the circuit design stage in which simultaneous impedance and noise matching is pursued.

That is, transistor has a characteristic dimension, the characteristic dimension being an emitter length l_E for a bipolar transistor and a gate width w_g for field effect transistor, which is designed to provide that the real part of its optimum noise impedance is equal to the characteristic impedance of the system, Z_O.

The first stage is dependent on the availability of scalable models, which have not until recently been available in the literature. Indeed, the design approach requires a physically based scalable model for bipolar transistors, and accurate closed-form noise parameter equations suitable for circuit design. Designing a minimal passive impedance matching circuit comprising first and second inductors, comprises determining the inductance of an emitter inductor L_E to match the real part of the input impedance to Z_O, and then, determining the inductance of a base inductor L_B to simultaneously match the imaginary part of the input impedance and the noise impedance to 0Ω.

This design approach is unique in treating the transistor geometry as a design variable. In particular, a characteristic dimension of the transistor, i.e. the emitter length of a bipolar transistor, or the gate width of a field effect transistor is optimised to achieve noise matching of the transistor. The design methodology allows for simultaneous optimization of both the transistor parameters and the passive matching network component parameters.

The steps of stage I, i.e. designing a noise matched transistor comprise: determining an optimal noise current density J_{Q1} according to equations:

$$F_{MIN} = 1 + \frac{I_C}{V_T|Y_{21}|^2}\left(Re\{Y_{11}\} + \sqrt{\left[1 + \frac{2V_T|Y_{21}|^2(r_E + r_B)}{I_C}\right]\left[|Y_{11}|^2 + \frac{I_B|Y_{21}|^2}{I_C}\right] - (Im\{Y_{11}\})^2}\right) \quad (1)$$

-continued

$$R_{sop} \equiv \frac{R_n f_T}{f} \frac{\sqrt{\frac{I_C}{2V_T}(r_E + r_B)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{4\beta_0 f^2}}}{\frac{I_C}{2V_T}(r_E + r_B)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2}{4}\left(1 + \frac{f_T^2}{\beta_0 f^2}\right)} = Z_0 \quad (2)$$

and determining the optimized emitter length l_E, by running a simulation using a scalable model to bias the transistor at the optimal noise density and adjust l_E until $R_{SOP}(I_E)=Z_0$ the characteristic impedance of the circuit, thereby determining the transistor size and bias current. Thus, the optimal noise current density is determined by using F_{MIN} vs. $\log(I_C)$ curves.

Preferably, the design is carried out using a commercially available design tool such as HSPICE™. The scalable models provide analytical equations for determination of the noise and impedance parameters of the transistors and passive components using a standard design tool. These equations were used to develop customised input decks for HSPICE to derive the required design parameters. Sample input decks developed for HSPICE for either bipolar transistors or MOSFETs are included in Appendices A and B, respectively. Alternatively appropriately customised decks to solve the equations may be created for other design tools. Thus optimized performance is readily obtainable with commercially available or custom design tools.

Thus, optimized noise and impedance matching of an integrated circuit is achieved in a integrated circuit of simple design by a two stage design approach providing a noise optimized transistor and a minimal inductor network for impedance matching. A simple transistor-inductor structure implemented in silicon, which is simultaneously noise and impedance matched. This structure is advantageously used to provide silicon implementations of LNA and double balanced mixer circuits with high frequency performance previously only reported for similar circuit implemented with III-V based technology.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a circuit schematic of part of a monolithic silicon integrated circuit comprising a transistor-inductor structure according to a first embodiment of the present invention;

FIG. **2** shows a circuit-schematic of part of a monolithic silicon integrated circuit comprising a transistor-inductor structure according to a second embodiment of the present invention;

FIG. **3** shows a circuit schematic of part of a monolithic silicon integrated circuit comprising a transistor-inductor structure according to a third embodiment of the present invention;

FIGS. **4** to **8** represent sequential steps in the design flow for the transistor-inductor structure of the first embodiment, i.e.

FIG. **4** shows graphical plot of the dependence of the noise parameter F_{MIN}, and transistor parameters f_T and f_{MAX}, on the collector current I_C of the transistor, from which, for a given transistor geometry $l_E >> w_E$, and bias voltage V_{CE}, the optimal noise current density J_C is derived at a desired frequency ω_T;

FIG. **5** shows a graphical plot of the emitter length l_E as a function of noise parameters F_{MIN}, F_{50} and the optimal source impedance R_{sop}, from which the emitter length is adjusted to set $R_{sop}(l_E)$ equal to the characteristic impedance of the system Z_0, typically 50Ω, to achieve noise matching of the transistor;

FIG. **6** shows the optimum noise impedance of the transistor plotted on a Smith chart at the end of the transistor design stage;

FIG. **7** represents the low noise circuit design flow step of adding an emitter inductor L_E to match the real part of the input impedance to Z_0;

FIG. **8** represents the low noise circuit design flow step of adding a base inductor L_B to simultaneously match the imaginary part of the input impedance and noise impedance to 0Ω;

FIG. **9** shows a circuit schematic of a LNA (core) circuit according to a fourth embodiment of the present invention;

FIG. **10** shows a circuit core schematic of a double balanced mixer (core) circuit according to a fifth embodiment of the present invention;

FIG. **11** shows measured values for the conversion gain and input and output return loss for the low noise amplifier circuit of the fourth embodiment;

FIG. **12** shows measured values for the conversion gain and input return loss for the mixer circuit of the fifth embodiment;

FIG. **13** shows the measured noise figure F_{MIN} as a function of frequency for the low noise amplifier circuit noise and impedance matched for 5.8 GHz;

FIG. **14A** shows a photomicrograph layout of the low noise amplifier circuit of the fourth embodiment;

FIG. **15A** shows a photomicrograph layout of the mixer circuit of the fifth embodiment;

FIG. **16A** shows a photomicrograph layout of a gain bandwidth and input impedance optimised Darlington amplifier (16 dB gain at 8 GHz designed using the scalable model;

FIG. **17A** shows a photomicrograph layout of a noise and impedance optimised Darlington amplifier (8 dB gain at 14 GHz) designed using the scalable model;

FIG. **18** shows the measured gain and input return loss of a 12.6 GHz bandwidth silicon Darlington amplifier; and

FIG. **19** shows the measured gain and group delay ripple of the 12.6 GHz bandwidth Darlington amplifier.

DESCRIPTION OF THE EMBODIMENTS

Part of a monolithic silicon integrated circuit **10** comprising an integrated transistor-inductor structure **12** according to a first embodiment of the present invention is shown schematically in FIG. **1**, and comprises a first transistor **14**, which is a common emitter bipolar transistor Q_1 for low noise amplification, and a second transistor **16**, which is a common base transistor Q_2 for input/output buffering, the two transistors being coupled in cascode configuration; a first inductor **18** L_E is coupled to the emitter **20** of the first transistor Q_1; and, a second inductor **22** L_B coupled to the base **24** of the first transistor Q_1. Noise and impedance matching of the transistor-inductor structure is achieved by designing the transistor **14** having an specific geometry, and in particular a specific emitter length l_E, which provides that

the real part of its optimum noise impedance at the desired frequency of operation and collector current density is equal to the characteristic impedance Z_0 of the system, i.e. the integrated circuit Once the transistor geometry is determined to provide noise matching, design of the matching network is reduced to adding a very simple passive matching network using only two inductors. The first inductor **20**, L_E, provides matching of the real part of the input impedance, and the second inductor **22**, L_B cancels out the noise reactance and input impedance reactance of the structure. Specifically the inductance values are determined to be $L_E=Z_O/\omega_T$, and $L_B=1/\omega^2C_{in}-L_E$.

The size ratio of the emitter lengths of the first and second transistors is determined by the ratio of the f_T current density to the minimum noise current density. In the circuit represented in FIG. **1**, the ratio is 8 to 1, which is technology dependent.

Thus an integrated transistor-inductor structure comprising a transistor Q1 having an emitter length l_E designed to provide noise matching at a desired operating frequency, and a simplified matching network of two inductors L_E and L_B of the appropriate values to provides impedance matching of the circuit, provides a simultaneously noise and impedance matched circuit. This structure is particularly advantageous in optimising performance of silicon based circuits for wireless and RF applications.

The design of the transistor-inductor structure is based on a design methodology, i.e. a method of designing an integrated circuit according to another aspect of the present invention, which will be described in detail in the following section, and in which the geometry of the transistor is determined by design, i.e. considered to be a variable rather than fixed design parameter. That is, the emitter length of a bipolar transistor, or correspondingly, the gate width of a field effect transistor (FET), is adjusted so that the transistor is noise matched to the characteristic impedance of the system, typically 50Ω, at the desired operating frequency, thereby minimizing the losses in the passive network around the transistor. Since the transistor is an active device, noise matching is achieved without losses and without noise figure degradation. The task of noise matching is thus removed from the passive network. The resulting matching network is therefore simpler, and less lossy than in presently known circuit designs.

To complete the noise and impedance matched transistor structure, a minimal passive network comprising two lossless integrated inductors is designed to provide impedance matching with the lowest possible degradation of the overall noise figure. The minimal matching network, reduces components and saves area, and therefore contributes to significant cost reduction.

Optimization and design of the integrated transistor-inductor structure of the circuit is possible only by the availability of scalable models for transistors, as described in a reference co-authored by the present-inventors, entitled "A scaleable high frequency noise model for bipolar transistors with application to optimal transistor sizing for Low noise amplifier design" to be published at the Bipolar Circuits and Technology Meeting, 30 Sep., 1996, which is incorporated herein by reference. The scalable models provide analytical equations describing noise parameters, as a function of the optimal noise current density J_{Q1}.

As described in this reference, a series of three equations were derived, defining the noise resistance R_n, optimum source admittance, Y_{SOP}, and minimum noise figure F_{MIN}, as functions of the shot noise current sources, transistor Y parameters, series emitter resistance r_E, and the total base resistance R_B. The bias current dependence of the noise parameters appears in explicit form via terms in I_B and I_C, and also implicitly in r_B and in the Y parameters. In derivation of these equations, it was assumed that the base and collector noise currents are uncorrelated. This is a reasonable simplification given the different physical origins of the two noise currents.

For bias current and frequency ranges used in wireless design, the model reduces to the following simplified yet accurate equations

$$F_{MIN}=1+\frac{I_C}{V_T|Y_{21}|^2}\left(Re\{Y_{11}\}+\sqrt{\left[1+\frac{2V_T|Y_{21}|^2(r_E+r_B)}{I_C}\right]\left[|Y_{11}|^2+\frac{I_B|Y_{21}|^2}{I_C}\right]-(Im\{Y_{11}\})^2}\right) \quad (1)$$

$$R_{sop}\equiv\frac{R_nf_T}{f}\;\frac{\sqrt{\frac{I_C}{2V_T}(r_E+r_B)\left(1+\frac{f_T^2}{\beta_0f^2}\right)+\frac{n^2f_T^2}{4\beta_0f^2}}}{\frac{I_C}{2V_T}(r_E+r_B)\left(1+\frac{f_T^2}{\beta_0f^2}\right)+\frac{n^2}{4}\left(1+\frac{f_T^2}{\beta_0f^2}\right)}=Z_0 \quad (2)$$

$$L_E\equiv\frac{Z_0}{2\pi f_T} \quad (3)$$

$$X_{sop}\equiv\frac{\frac{nR_nf_T}{2f}}{\frac{I_C}{2V_T}(r_E+r_B)\left(1+\frac{f_T^2}{\beta_0f^2}\right)+\frac{n^2}{4}\left(1+\frac{f_T^2}{\beta_0f^2}\right)}-2\pi fL_E \quad (4)$$

$$L_B\equiv\frac{1}{\omega^2C_{in}}-L_E \quad (5)$$

These equations can be employed to tailor the device size. Typically, for a bipolar transistor, it is required only to optimize the emitter length l_E to achieve optimal low noise performance and minimum matching network losses. Once a noise matched transistor is obtained, impedance matching is achieved very simply by selecting appropriate values for the two inductors L_E and L_B as defined by equations 3 and 5. These two inductors are the only required passive components used for impedance matching. The structure is compact, and the minimal impedance matching circuit contributes significantly to reducing possible degradation of the overall noise figure of a monolithically integrated transistor-inductor structure.

As indicated by equations (1) and (2), the noise resistance and the optimum noise admitttance scale as l_E and l_E^{-1},

respectively. β is the dc current gain and n is the collector current ideality factor, typically n=1.

F_{MIN} of the transistor is invariant to changes in emitter length provided that the length to width ratio l_E/w_E of the emitter stripe is greater than 10.

All noise parameters are non-linear functions of emitter width, w_E through the $I_C(r_E+r_B)$ term. The ability to predict the impact of the statistical emitter width and length variations on the noise parameters depends on the availability of a physically based, scalable compact model.

While noise parameters are available from the post processor of microwave circuit simulators such as LIBRA, only equivalent noise voltages and currents can be modelled directly using SPICE like simulators. Thus customised HSPICE input decks were developed, based on equations 1 to 3, to compute simultaneously F_{MIN}, f_T, F_{MAX}, R_n and Y_{sop} as functions of I_C in a single simulation run. The HSPICE calculated noise parameters were found to agree within 0.25 dB up to 10 GHz with those generated by LIBRA.

For the combination of the first transistor and the two inductors, a unique combination of l_{E1}, J_{Q1}, L_E and L_B is determined that leads to a structure with minimum noise figure F_{MIN} and ideal input impedance match. While the second transistor is optional and may be omitted, for practical purposes the second transistor is included in order to maximize the power gain and the frequency of operation. The size of the second transistor Q2 is selected such that it is biased at the current density at which its cut-off frequency reaches a maximum. The size ratio of Q1 to Q2 depends on the ratio of the peak f_T current density to the minimum noise current density.

In practice, the design of a noise and impedance matched circuit is achieved in two stages, I) the noise matched transistor design stage and II) the circuit design stage in which simultaneous impedance and noise matching is pursued.

Based on the scalable model described in the above mentioned reference, the first stage of the design process involves finding the optimal noise current density, from an analytic equation as set out below, using a commercial design tool, i.e. HSPICE.

The noise parameter equations set out in the references, in analytical format were entered in an HSPICE simulator input deck to compute simultaneously the minimum noise figure F_{MIN}, the cut-off frequency f_T, maximum oscillation frequency f_{MAX} noise resistance R_n, and optimum source admittance Y_{SOP} as functions of the transistor collector current I_C for a bipolar transistor, (or correspondingly, as functions of transistor drain current I_D when a MOSFET transistor is to be considered). Corresponding sample HSPICE decks for a bipolar and MOSFET transistor are given in the appendices A and B respectively.

The design of the optimized structure of FIG. 1, based on a bipolar transistor, is described in the following example:

Stage I

The optimal noise current density J_{Q1} is obtained from equation (1) using an HSPICE deck, as represented in FIG. 4, which shows graphically the dependence of F_{MIN}, f_T and f_{max} on the collector current. From this data, the optimal noise current density J_{Q1} is determined for the desired operating frequency. Since R_{sop} is a function of l_E, the emitter length, this parameter is adjusted so that the optimum source resistance R_{SOP} equals the characteristic impedance of the system Z_O (50Ω) at the minimum noise current density and at frequency f, as expressed in equation (2), which is represented graphically in FIG. 5.

By these two steps, the transistor size, specifically l_E and bias current are determined. The optimum noise impedance of the transistor at the end of the first stage is shown plotted on a Smith chart in FIG. 6.

Stage II

Once the optimized geometry of the noise matched transistor is determined, an emitter inductor L_E is added to match the real part of the input impedance to Z_O as shown in FIG. 7, and defined by equation (3) as a function of the frequency f_T.

If lossless, L_E does not change the value of R_{SOP} but it does affect the source reactance X_{SOP} which is defined by equation (4). Finally, simultaneous noise and input impedance matching is obtained by connecting an inductor L_B in the base of the transistor Q1 as shown in FIG. 8. This inductor cancels out the reactance due to the input capacitance, C_{in}, of the device, and at the same time, it transforms the optimum noise reactance of the amplifier to 0Ω. L_B is defined by equation (5).

In essence, this design methodology ensures that the real part of the optimum noise impedance of the transistor is equal to the characteristic impedance Z_O at desired frequency and collector current density.

Optimal noise and input impedance matching is achieved with the simplest matching network. Optionally, a suitable matching network in the collector may be added to maximize the power gain. The scaleable model allows for the transistor size to be uniquely dimensioned in order to achieve optimal noise matching. The optimal transistor size and bias current decrease with increasing frequency.

This approach differs significantly from conventional designs in which the transistor size is not a design variable, but a fixed parameter which cannot be optimized by a circuit designer. A scaleable noise model has not previously been available in the literature. Conventional circuit design for low noise has relied on time consuming trial and error processes.

Single transistor test structures with emitter inductors only, and with both base and emitter inductors were fabricated in a proprietary Northern Telecom silicon bipolar process (NT25) at 1.9, 2.4 and 5.8 GHz. As described in the above mentioned reference to Voinigescu, test structures were fabricated with various emitter widths, lengths, and single and multistripe geometries. Agreement between measured parameters and Spice Gummel Poon modelled parameters were well within the typical on wafer noise measurement error.

Measured data confirmed the simultaneous noise and impedance match. The input return loss was better than −19 dB in all examples. The finite Q of the fabricated inductors on silicon substrates was typically in the range from 7 to 10, degrading the noise figure by 0.7 to 1.4 dB. It was found that the base inductor contributed 0.4 to 0.7 dB to the measured overall noise figure.

Part **40** of a monolithic silicon integrated circuit operable as a differential amplifier according to a second embodiment of the present invention is shown schematically in FIG. 2. This circuit is the differential equivalent of the single ended amplifier structure **10** shown in FIG. 1. Thus, the circuit **40** comprises an input pair **42** and **44** of common emitter bipolar transistors Q1 and Q2 for low noise amplification, and an output pair **46** and **48** of common base bipolar transistors Q3 and Q4 for input/output buffering, the two pairs being coupled in cascode configuration. Inputs for supplying differential RF signals RF_N and RF_P are coupled to the emitters of the input pair Q1 and Q2, and differential output signals OUT_P and OUT_N generated at outputs coupled to the collectors of output pair Q3 and Q4. Matching of the real part of the noise impedance of the input pair of

transistors Q1 and Q2 is achieved as described for the single ended structure of the first embodiment, by design of the transistors Q1 and Q2 with appropriate an emitter length to make the real part of its optimum noise impedance at the desired frequency of operation and collector current density equal to the characteristic impedance Z_O.

It may be shown that the minimum noise figure of a differential amplifier stage is identical to that of a single ended amplifier stage. Consequently, the size of each of the transistors, i.e. the emitter length l_{E_D} of the input pair Q1 and Q2 of the differential amplifier is roughly twice as large as that of the single ended stage. Therefore, the emitter length is indicated as $l_{E_D}=2\times l_E$ where l_E is the emitter length of the input transistor of the corresponding single ended circuit shown in FIG. **2**. Emitter inductors **50** and **52**, L_E and L_E', provide matching of the real part of the input impedance and base inductors **52** and **54**, L_B and L_B', cancel out the noise reactance and input impedance reactance of the structure, as described for the structure of the first embodiment, to complete noise and impedance matching. Specifically the inductance values are determined to be $L_E=Z_O/\omega_T$, and $L_B=1/\omega^2C_{in}-L_E$. Analogously, the ratio of the sizes of the first and second pairs of transistors, i.e. emitter lengths of the Q1 and Q2, relative to the emitter lengths of Q3 and Q4, is by the ratio of the peak f_T current density to the minimum noise current density, as determined for the single ended amplifier. Thus the emitter lengths of Q3 and Q4 are ⅛ of the emitter length l_{E_D} of the input pair Q1 and Q2, or as shown in FIG. **2**, as $l_E/4$ where l_E is the emitter length of the input transistor of the corresponding single ended circuit shown in FIG. **1**.

Part of a monolithic silicon integrated circuit **100** operable as a mixer circuit and comprising an integrated transistor-inductor structure **110** according to a third embodiment of the present invention is shown schematically in FIG. **3**, and comprises a first transistor **112**, which is a common emitter bipolar transistor Q_1 for low noise amplification, and a second transistor **114**, which is a common base transistor Q_2 for mixing, the two transistors **116** L_E is coupled to the emitter **118** of the first transistor Q_1; and, a second inductor **120** L_B coupled to the base **120** of the first transistor Q_1. An RF signal is supplied to an input coupled to the base of the first transistor Q1 through L_B, and an LO input signal are supplied to an input coupled to the base **124** of the second transistor Q2 through another base inductor **126** L_{B2}, thereby generating an IF output signal at an output coupled to the collector **128** of the second transistor Q2. As in the low noise amplifier configuration of the first embodiment, noise and input impedance matching of the transistor-inductor structure is achieved by designing the transistor **112** having an specific geometry, and in particular a specific emitter length l_E, which provides that the real part of its optimum noise impedance at the desired frequency of operation and collector current density is equal to the characteristic impedance Z_O of the system, i.e. the integrated circuit. Once the transistor geometry is determined to provide noise matching, design of the matching network is reduced to adding a very simple passive matching network using only two inductors. The first inductor L_E, provides matching of the real part of the input impedance, and the second inductor L_B cancels out the noise reactance and input impedance reactance of the structure. Specifically the inductance values are determined to be $L_E=Z_O/\omega_T$, and $L_B=1/\omega^2C_{in}-L_E$. The size ratio of the transistor Q1 and Q2, i.e. the ratio of the emitter lengths of the first and second transistors, is determined by the ratio of the peak f_T current density to the minimum noise current. In this example the emitter length ratio was 8:1, which is technology dependent.

To demonstrate the performance improvements achieved in application of the matched transistor-inductor structure, two silicon integrated circuits were designed, a double balanced mixer and a low noise amplifier, for application in a 5.8 GHz down-converter. The two circuits were designed to be simultaneously noise and impedance matched at the RF input, and were fabricated in a proprietary Northern Telecom 25 GHz silicon bipolar process technology (NT25) using implanted base, double polysilicon transistors, inductors, and microstrip transmission lines. The three layer metallization with 2 μm thick aluminum top metal layer allows for the fabrication of inductors with Q's in the 6–10 range, and of metal **1** grounded microstrip lines with Qs of 6, at 26 GHz. Transistors have f_T and f_{MAX} of 24 GHz and 38 GHz respectively at V_{CE}=1V. NF_{MIN} is typically 2 dB at 5.8 GHz and BV_{CEO} and BV_{CBO} are 4.2V and 15V respectively.

A schematic of the core of a silicon double balanced mixer circuit according to a fourth embodiment of the present invention is shown in FIG. **9**. The circuit is a development based on a CDMA GaAs MESFET mixer architecture described in the Brunel reference, which is is a modified Gilbert cell mixer incorporating an inductor/capacitor/resistor matching network. The circuit shown in FIG. **9** differs in incorporating the noise and impedance matched transistor-inductor structure, which simplifies the matching network, as described above, and allows for implementation in silicon with performance comparable to GaAs at 5.8 GHz. The mixer comprises an input pair of common emitter transistors Q1 and Q2, each coupled to respective common source differential pairs Q3, Q4 and Q5, Q6 which form a mixing quad. Differential RF inputs are coupled to the bases of the input pair, and differential LO inputs are coupled to the bases of differential pairs of the mixing quad to generate differential IF output signals at outputs coupled to collectors of the pairs the mixing quad.

The emitter lengths of Q1 and Q2 are designed to provide matching of the real part of the noise impedance, and first and second inductors provide a passive matching network, as described above. Thus, the emitter inductors L_E and L_E' provide matching of the real part of the input impedance to Z_O. The base inductor L_B provides for cancelling the imaginary part of the input impedance and the noise reactance. Since one of the RF inputs is AC grounded, a single base inductor L_B only is required. The mixer also features an LO reject, series LC filter between the differential IF outputs, and a parallel LC resonator, tuned on the second RF harmonic, as an AC current source in the emitter of the input pair.

Inductors, L_E, replace conventional resistors for emitter degeneration. The inductors alleviated to a large degree the trade off between IIP3 and the noise figure. However, since the input third order intercept point, IIP3, is proportional to $\omega g_m L_E$ and, since for ideal input match $L_E=Z_O/2\pi f_T$, IIP3 and input matching become intertwined, that is, $IIP3\sim\omega g_m Z_O/2\pi f_T$.

In integrated circuit implementations, Z_O can usually be increased from the typical 50Ω, if required, in order to further improve IIP3.

A silicon low noise amplifier (LNA) circuit according to a fifth embodiment is shown in FIG. **10**, and has an architecture similar to that usually implemented in GaAs circuits. The circuit differs in that it incorporates the simultaneously noise and impedance matched transistor-inductor structure comprising bipolar transistor Q1, and inductors L_E and L_B, as described in the first embodiment, and is implemented in silicon for operation at 5.8 Ghz.

As shown in FIG. **10**, the first transistor Q_1 is a 2×0.5*20 m^2 bipolar device, biased at a minimum noise current of 2.2 mA. This is different from the mixer circuit of the fourth embodiment, which is fully differential. It can be demonstrated that the minimum noise figure of a differential stage is identical to that of the half circuit and that the optimum noise impedance is two times larger. As a result, the size of each of the transistors in the input pair of the double balanced mixer of FIG. **9** is 4×0.5*20 μm^2 and bias current is 4 mA, roughly twice those of the LNA (FIG. **10**). Both circuits are noise and input impedance matched to 50Ω. In order to maximize gain and bandwidth, the size of the transistors in the mixing quad was chosen 8 times smaller than that of the input pair, as indicated in the basic transistor-inductor structure shown in FIG. **1**. The size ratio corresponds to the ratio of the peak f_T current density and the minimum noise current density. A similar approach is used for common base transistor Q2 in the LNA to increase gain by 1 to 2 dB.

Schematic layouts of the integrated circuits for the LNA and double balanced mixer circuits are shown in FIGS. **14** and **15**. Corresponding photomicrographs of the actual integrated circuit layouts, on a reduced scale, are shown in FIGS. **14A** and **15A**. 50Ω microstrip transmission lines with metal 1 ground planes were used at the local oscillator inputs, in order to minimize substrate losses and to provide a controlled and dispersion free transmission medium.

The measured performance of the LNA and double balanced mixer are summarized in Table 1 for operation at 5.8 GHz. The gain and input return loss of the LNA mixer are shown in FIG. **11** and **12** respectively. The noise figure for the 5.8 GHz LNA is plotted vs. frequency in FIG. **13**. The conversion gain of the mixer was measured with a noise figure meter and was confirmed with S parameter measurements with the mixer biased as an amplifier with dc LO inputs only.

TABLE 1

	S_{21}	NF	S_{11}	IIP3	V_{cc}	PD
LNA	7.2 dB	4.2 dB	−35 dB	−4 dBm	3.5 V	7.7 mW
Mixer	21 dB	4.2 dB	−22 dB	−2 dBm	3.3 V	26 mW

The mixer and LNA circuits of the fourth and fifth embodiments were based on silicon bipolar transistors.

Alternatively, these circuits may be implemented using silicon MOSFET transistors. The scalable model for bipolar transistors mentioned above is adaptable to silicon MOSFETs. For silicon MOSFETs, the scalable MISNAN model, developed by Northern Telecom Limited is employed.

Thus analogous MOSFET based circuits similar to those described above, except that the bipolar transistors are replaced with appropriately designed, noise matched silicon MOSFETs. Test measurements on the performance of MOSFET based circuits are not yet available. A sample HSPICE input deck for Silicon MOSFETs is given in Appendix B.

The resulting analytical expressions for the noise parameters of both bipolar and MOSFET devices allow for the design of the transistor geometry to achieve noise matched devices at a given frequency f, and system impedance Z_0.

The inventors believe, to the best of their knowledge, that the LNA and mixer circuits described herein are the first fully integrated silicon based mixer and low noise amplifier circuits which have been demonstrated to be operable at 5.8 Ghz, with performance which has previously only been achieved using GaAs based circuits. Moreover, the circuits occupy a record small area for a LNA and a mixer circuit, and provide a factor of at least two in cost reduction relative to a comparable GaAs implementation delivering similar performance.

The noise and impedance matched inductor-transistor structure may also be used for other RF and wireless circuits.

The availability of the scalable models and the analytical noise parameter equations have opened up a new design philosophy for radio frequency (RF) integrated circuits and microwave monolithic integrated circuits (MMICs).

For example, test results showed improved performance when the scalable model was applied to the design of silicon based Darlington amplifiers having 16 dB gain, 7.1 GHz bandwidth and 8 dB gain 12.6 GHz bandwidth, the layouts of which are shown schematically in FIGS. **16** and **17**. Corresponding photomicrographs of the chip layout on a reduced scale are shown in FIGS. **16A** and **17A**. These circuits would have potential applications in broadband optical fiber transmission at 10 Gb/s and 17.5 Gb/s respectively. The size of the output transistor was selected to meet the output compression point specification whereas the input transistor length was optimized to reduce the group delay ripple within the 3 dB bandwidth by adjusting the Q of the resonant circuit associated with the negative resistance of the emitter-follower. The series and shunt feedback resistor values were designed to meet the gain and low frequency input match specification. On-chip input inductors were employed to improve the input return loss at high frequencies. The measured performance is summarized in Table 2.

TABLE 2

Band	S_{21}	S_{11}	delay	P_{1dB}	V_{cc}	PD
12.6 GHz	7.8 dB	−30 dB	8 ps	−12 dBm	3.3 V	0.12 W
7.1 GHz	16 dB	−22 dB	8 ps	−16 dBm	3.3 V	0.16 W

The gain input return loss and group delay are plotted in FIGS. **18** and **19** as functions of frequency for the 12.6 GHz bandwidth Darlington amplifier. The noise figure of the 7.1 GHz Darlington amplifier is 5.7 dB at 2 GHz increasing to 8.17 dB at 7 GHz. The 12.6 GHz Darlington amplifier has a noise figure of 7.1 dB and 12.5 dB at 2 GHz and 12 GHz respectively.

Gain and bandwidth variation across the wafer for the 8 dB gain amplifier was better than 0.8 dB and 1 GHz respectively.

In summary, the design methodology for the noise and input impedance matched transistor-inductor structure is based on two key features. First, the transistor geometry is treated as a design variable to achieve matching of the real part of the noise impedance of the transistor to the characteristic impedance at the desired frequency, i.e. by adjusting the emitter length or gate width. This approach is in contrast to conventional designs in which the transistor dimensions (size) are treated as fixed parameters. Thus the transistor size is selected initially to suit the application. Second, a minimal passive network is then designed around the noise matched transistor. Again, this contrasts with the conventional approach in which a relative complex passive network is required to provide noise and impedance matching. A conventional matching network is therefore considerably more lossy and occupies a much larger area than the relatively simple matching network resulting from the methodology described herein.

Circuit performance is optimized using fewer components, and the integrated circuit chip area is reduced, both factors being significant cost drivers in integrated circuit manufacturing.

Thus, fabrication of highly cost effective, high performance silicon integrated circuit for RF and wireless applications in the 5 to 6 GHz band is demonstrated to be feasible. The inventors believe that this is a record high frequency for a silicon integrated mixer and LNA circuit circuits. This achievement was made possible only by the used of the design philosophy described herein, together with a high speed silicon bipolar process with integrated is inductors. Improved performance of the circuits is also achieved by the use of the triple level metal process to provide a low loss metal 3 microstrip transmission line structure, using silicon dioxide dielectric, and metal 1 ground planes.

The transistor size for optimal noise match depends on operating frequency and bias current density, whether the circuit is implemented in silicon bipolar technology, i.e. either bipolar junction transistors (BJTS) or Heterojunction bipolar transistors (HBTs); or field effect transistors, MOSFET, MESFET, JFET, HEMT. Sample HSPICE input decks for both bipolar and MOSFET transistors may be adapted for these transistors. The design methodology is particularly applicable to optimising noise and input impedance to reduce losses significantly, and obtain optimal performance in integrated circuits designed in silicon or using heterostructures such as silicon-germanium. Nevertheless, the methodology is also useful in overcoming the trade-off in noise and input impedance matching to improve performance in HBTs, using GaAs, InP and other compound semiconductor integrated circuits.

Furthermore, while simulations based on HSPICE are described in detail, other commercially available or custom design tools may be used.

While specific embodiments have been described in detail, it will be appreciated that variations and modifications to these embodiments may be made within the scope of the following claims.

APPENDICES

APPENDIX A: HSPICE INPUT DECK FOR BIPOLAR TRANSISTORS

```
Fin (@5.8 GHz), fT, fMAX vs log(Ic)
*This Hspice input deck generates .mai output files
*tabulating NF, fT, Fmax, noise resistance NRn, optimum source
*conductance NGop,
*optimum source susceptance Nbop, and S parameters required for
associate gain,
*all as functions of the collector current.
*the effect of series parasitics rs, lss, re, le can also be studied.
*three different NT25 transistors are simulated here to investigate
noise
*figure scaling.
*reb = RE + RBX + series parasitics.
*1 × 2(X1.Q) is the collector current
*1/1 × 16(X1.Q) is the internal base resistance
*tv2 = 2*VT
*
*For reference: Sorin Voinigescu x34574
*
*
.OPTION nopage autostop search = ' '
.OPTION INGOLD = 1
*.OPTION ABSVAR = .025 DVDT RELVAR = 0.05 NEWTOL
.OPT POST = 2 ** hsplot plot format
.OPTIONS DCAP = 1
.TEMP = 23 TNOM = 23
.PARAM jbase = 8e5 vce = 1.0
vce ext_c 0 vce
ibase 0 ext_b ac = 1 dc = ibase
.param rs = 0.0 lss = 0.0e − 11 re = 0.0 le = 0.0e − 11 cp = 0.0e − 14
.param emitter_width = unif(0.5u, 0.2)
.param length = 10u
x1 c b e e nt25npn
+              new = emitter_width nel = length
+         nestripes = 1 nbstripes = 1 ncstripes = 1
+         dtemp = 0
.param area = 'length*emitter_width' ibase = 'jbase*area'
* parasitics
rbb int_b b rs
ree int_e e re
rcc int_c c rs
lbb ext_b int_b lss
lee int_e 0 le
lcc ext_c int_c lss
cin ext_b 0 cp
cout ext_c 0 cp
.op
.NET i(vce) ibase ROUT = 50 RIN = 50
.ac dec 10 0.1G 60G
* + SWEEP MONTE = 30
+ sweep jbase poi 23 1e5 1.5e5 2e5 3e5 4e5 6e5 7e5 8e5
+ 9e5 1e6 1.5e6 2e6 3e6 4e6 6e6 8e6 1e7 1.5e7 2e7 3e7 4e7 6e7 8e7
* + sweep vce poi 3 1 2 3
*
```

APPENDICES-continued

APPENDIX A: HSPICE INPUT DECK FOR BIPOLAR TRANSISTORS

```
* + sweep length poi 6 5u 10u 15u 20u 25u 30u
* + sweep emitter_width poi 10 0.3u 0.4u 0.5u 0.6u 0.7u 0.8u 0.9u 1.0u
1.1u 1.2u
*
.param tv2 = 0.0516
+ reb = '1v2(X1.RE) + LV2(X1.RBX) + rs + re'
+ Rn = 'reb + 1/1 × 16(X1.Q) + 1 × 2(X1.Q)/tv2/(y21(m)**2)'
+
Gcore = 'y11(r)*1 × 2(X1.Q)/((reb + 1/1 × 16(X1.Q))*tv2*(y21(m)**2) + 1 × 2(X1.Q))
'
+
Bcor = 'y11(i)*1 × 2(X1.Q)/((reb + 1/1 × 16(X1.Q))*tv2*(y21(m)**2) + 1 × 2(X1.Q))
'
+Gopt = 'sqrt(((y11(m)**2)*1 × 2(X1.Q) + (y21(m)**2)*ibase)/(1 × 2(X1.Q) + tv2*
(reb + 1v14(X1.Q))*(y21(m)**2)) −
(y11(i)*1 × 2(X1.Q)/((reb + 1/1 × 16(X1.Q))*tv2*y21(m)**2) + 1 × 2(X1.Q)))**2)
'
+
nfmin = '10*log10(1 + 2*1 × 2(X1.Q)/tv2/(y21(m)**2)*(y11(r) + sqrt((1 + (reb + 1/
1 × 16(X1.Q))*tv2*(y21(m)**2)/1 × 2(X1.Q))*(y11(m)**2 + ibase/1 × 2(X1.Q)*(y2
1(m)**2)) − y11(i)**2)))'
.print ac Rn = par('reb + 1/1 × 16(X1.Q) + 1 × 2(X1.Q)/tv2/(y21(m)**2)')
+
Gcor = par('y11(r)*1 × 2(X1.Q)/((reb + 1/1 × 16(X1.Q))*tv2*(y21(m)**2) + 1 × 2(X1
.Q))')
.print ac
+
Gopt = par('sqrt(((y11(m)**2)*1 × 2(X1.Q) + (y21(m)**2)*ibase)/(1 × 2(X1.Q) + t
v2*(reb + 1v14(X1.Q))*(y21(m)**2)) −
y11(i)*1 × 2(X1.Q)/((reb + 1/1 × 16(X1.Q))*tv2*(y21(m)**2) + 1 × 2(X1.Q)))**2)
')
+ Bopt = par(' −
y11(i)*1 × 2(X1.Q)/((reb + 1/1 × 16(X1.Q))*tv2*y21(m)**2 + 1 × 2(X1.Q))')
.print ac
+
nfmin = par('10*log10(1 + 2*1 × 2(X1.Q)/tv2/(y21(m)**2)*(y11(r) + sqrt((1 + (re
b + 1/1 × 16(X1.Q))*tv2*(y21(m)**2)/1 × 2(X1.Q))*(y11(m)**2 + ibase/1 × 2(X1.Q)
*(y21(m)**2)) − y11(i)**2)))')
.MEASURE 'ic'      find 1 × 2(X1.Q) at 5.8G
.MEASURE 'jc' find par('1 × 2(X1.Q)*ie − 9/area') at 5.8G
.MEASURE 'one_ic' find par('1/1 × 2(X1.Q)') at 5.8G
.MEASURE 'NRn'      find
par('(reb + 1/1 × 16(X1.Q) + 1 × 2(X1.Q)/tv2/(y21(m)**2))/50') at 5.8G
.MEASURE 'Ngcor'      find
= par('y11(r)*1 × 2(X1.Q)/((reb + 1/1 × 16(X1.Q))*tv2*(y21(m)**2) + 1 × 2(X1.Q))
')
+ at 5.8G
.MEASURE 'Ngop'      find
+
par('sqrt(((y11(m)**2)*1 × 2(X1.Q) + (y21(m)**2)*ibase)/(1 × 2(X1.Q) + tv2*(reb
+ 1v14(X1.Q))*(y21(m)**2)) −
(y11(i)*1 × 2(X1.Q)/((reb + 1/1 × 16(X1.Q))*tv2*(y21(m)**2) + 1 × 2(X1.Q)))**2)
')
+ at 5.8G
.MEASURE 'Nbop'      find = par(' =
y11(i)*1 × 2(X1.Q)/((reb + 1/1 × 16(X1.Q))*tv2*(y21(m)**2) + 1 × 2(X1.Q))')
+ at 5.8G
.MEASURE 'NF'
+ find
+
par('10*log10(1 + 2*1 × 2(X1.Q)/tv2/(y21(m)**2)(y11(r) + sqrt((1 + (reb + 1/1 ×
16(X1.Q))*tv2*(y21(m)**2)/1 × 2(X1.Q))*(y11(m)**2 + ibase/1 × 2(X1.Q)*(y21(
m)**2)) − y11(i)**2)))')
+ at 5.8G
*.MEASURE 'beta'      find 1v10(X1.Q) at 5.8G
.MEASURE 'ftau2'      find par('h21(m)*2/sqrt(1 −
(h21(m)/1v10(X1.Q))**2)') at 2G
.MEASURE 'fT'      when h21(db) = 0
.MEASURE 'fmax'
+ WHEN par('s21(m)*s21(m)/(1 − s11(m)*s11(m))/(1 − s22(m)*s22(m))') = 1
.MEASURE 's11_r'      find s11(r) at 5.8G
.MEASURE 's11_i'      find s11(i) at 5.8G
.MEASURE 's21_r'      find s21(r) at 5.8G
.MEASURE 's21_i'      find s21(i) at 5.8G
.MEASURE 's12_r'      find s12(r) at 5.8G
.MEASURE 's12_i'      find s12(i) at 5.8G
.MEASURE 's22_r'      find s22(r) at 5.8G
```

APPENDICES-continued

APPENDIX A: HSPICE INPUT DECK FOR BIPOLAR TRANSISTORS

```
.MEASURE 's22_i'     find s22(i) at 5.8G
.LIB
'/bnr/users/bcrks2ef_1/sorinv/ProcessFiles/ta18/technology.nt25.nom'
nom
.inc '/bnr/users/bcrks2ef_1/sorinv/ProcessFiles/ta18/npn.subckt'
*
*.alt
*.LIB
'/bnr/users/bcrks2ef_1/sorinv/ProcessFiles/ta18/technology.nt25.worst
' worst
*.alt
*.LIB
'/bnr/users/bcrks2ef_1/sorinv/ProcessFiles/ta18/technology.nt25.best'
best
*
.END
```

APPENDIX B: HSPICE INPUT DECK FOR MOSFET TRANSISTORS

```
Fmin(@2.5GHz), fT, fMAX vs Ic
*Based on
*G.Dambrine et al., "A New Method for On Wafer Noise Measurement",
* IEEE-MTT, vol.41, pp.375–381, 1993.
.OPTION nopage autostop search = '   '
.OPTION INGOLD = 1
.OPTION ABSVAR = .025 DVDT RELVAR = 0.05 NEWTOL
.OPT POST = 2 ** hsplot plot format
.PARAM      vce = 2.5
.NET i(vce) vgs ROUT = 50 RIN = 50
vce ext_c 0 vce
vgs ext_b 0 ac = 1 dc = vgs
mft c b e e MNCH.0P8
+ L = LL
+ W = WW
+ AD = 5e − 11
+ PD = 8.3e − 05
+ AS = 5e − 11
+ PS = 8.3e − 05
* parasitics
.param rs = 5 ls = 5.0e − 11 re = 1.0 le = 2.0e − 11 cp = 0.0e − 14
rbb int_b b rs
ree int_e e re
rcc int_c c rs
lbb ext_b int_b ls
lee int_e 0 le
lcc ext_c int_c ls
cin ext_b 0 cp
cout ext_c 0 cp
.param WW = 32e − 05 LL = 8e − 07 vgs = 1 p = 0.666
.param reb = 'rs + re' area = 'WW*LL'
.op
.ac dec 10 0.1G 40G
* t × 10 bias
+ sweep vgs 0.5 3.5 0.1
*+ sweep vce poi 3 1 2 3
.param Rn = 'reb + p*1 × 7(mft)/(y21(m)**2)'
.param Gcor = 'y11(r)*p*1 × 7(mft)/((reb)*(y21(m)**2) + p*1 × 7(mft))'
.param Bcor = 'y11(i)*p*1 × 7(mft)/((reb)*(y21(m)**2) + p*1 × 7(mft))'
.param
Gopt = 'sqrt(((y11(m)**2)*p*1 × 7(mft))/(p*1 × 7(mft) + (reb)*(y21(m)**2)) −
*y11(i)*p*1 × 7(mft)/((reb)*(y21(m)**2) + p*1 × 7(mft)))**2)'
.param
+
nfmin = '10*log10(1 + 2*p*1 × 7(mft)/(y21(m)**2)*(y11(r) + sqrt((1 + (reb)*(y21
(m)**2)/p/1 × 7(mft))*(y11(m)**2) − y11(i)**2)))'
.print ac Rn = par('reb + p*1 × 7(mft)/(y21(m)**2)')
+ Gcor = par('y11(r)*p*1 × 7(mft)/((reb)*(y21(m)**2) + p*1 × 7(mft))')
.print ac
+
Gopt = par('sqrt(((y11(m)**2)*p*1 × 7(mft))/(p*1 × 7(mft) + (reb)*(y21(m)**2)
) − *(y11(i)*p*1 × 7(mft)/((reb)*(y21(m)**2) + p*1 × 7(mft)))**2)')
+ Bopt = par(' − y11(i)*p*1 × 7(mft)/((reb)*y21(m)**2 + p*1 × 7(mft))')
.print ac
+
nfmin = par('10*log10(1 + 2*p*1 × 7(mft)/(y21(m)**2)*(y11(r) + sqrt((1 + (reb)*
*y21(m)**2)/p/1 × 7(mft))*(y11(m)**2) − y11(i)**2)))')
.MEASURE 'id'      find 1 × 4(mft) at 2.5G
.MEASURE 'jd' find par('1 × 4(mft)/area') at 2.5G
.MEASURE 'gm' find par('1 × 7(mft)') at 2.5G
```

APPENDICES-continued

APPENDIX A: HSPICE INPUT DECK FOR BIPOLAR TRANSISTORS

```
.MEASURE 'NRn'      find par('reb + p*1 × 7(mft)/(y21(m)**2)') at 2.5G
.MEASURE 'Ngcor'    find
= par('y11(r)*p*1 × 7(mft)/((reb)*(y21(m)**2) + p*1 × 7(mft))')
+ at 2.5G
.MEASURE 'Ngop'     find
+ par('sqrt(((y11(m)**2)*p*1 × 7(mft))/(p*1 × 7(mft) + (reb)*(y21(m)**2)) -
(y11(i)*p*1 × 7(mft)/((reb)*(y21(m)**2) + p*1 × 7(mft)))**2)')
+ at 2.5G
.MEASURE 'Nbop'     find = par(' -
y11(i)*p*1 × 7(mft)/((reb)*(y21(m)**2) + p*1 × 7(mft))')
+ at 2.5G
.MEASURE 'NF'
+ find
+
par('10*log10(1 + 2*p*1 × 7(mft)/(y21(m)**2)*(y11(r) + sqrt((1 + (reb)*(y21(m
)**2)/p/1 × 7(mft))*(y11(m)**2) - y11(i)**2)))')
+ at 2.5G
.MEASURE 'fT'       when h21(db) = 0
.MEASURE 'fmax'
+ WHEN par('s21(m)*s21(m)/(1 - s11(m)*s11(m))/(1 - s22(m)*s22(m))') = 1
.MEASURE 's11_r'    find s11(r) at 2.5G
.MEASURE 's11_i'    find s11(i) at 2.5G
.MEASURE 'm_s21'    find s21(m) at 2.5G
*
*
.LIB '/bnr/ntcad.alpha/tech/nte/batmos/DK/hspice/nmos' TYPICAL
.END
```

What is claimed is:

1. An integrated circuit including an integrated transistor-inductor structure comprising:

a transistor having geometric dimensions comprising a characteristic dimension, the characteristic dimension being an emitter length, l_E for a bipolar transistor, and a gate width w_g for a field effect transistor, the characteristic dimension being selected to provide the real part of the optimum noise impedance equal to the characteristic impedance of the integrated circuit Z_O, thereby providing noise matching of the transistor at a selected operating frequency and bias current density;

and a passive matching network consisting of a first inductor for matching the real part of the input impedance to Z_O, and a second inductor for cancelling out the imaginary part of the input impedance and the noise reactance respectively, the circuit thereby providing simultaneous noise and input impedance matching.

2. A silicon integrated structure according to claim 1 wherein the first inductor $L_E=Z_O/\omega_T$, where ω_T is operational frequency and wherein the second inductor $L_B=1/\omega^2C_{in}-L_E$, wherein C_{in} is the total input capacitance of the transistor.

3. An integrated circuit according to claim 1 wherein

the transistor comprises a bipolar transistor comprising an emitter, base and collector, coupled in common emitter configuration, the length l_E of the emitter being optimized to provide noise matching of the transistor,

the first inductor being an emitter coupled inductor L_E for matching the real part of the input impedance Z_O, and the second inductor being a base coupled inductor L_B for matching the imaginary part of the input impedance and noise reactance to 0Ω.

4. An integrated circuit according to claim 1 wherein

the transistor comprises a silicon field effect transistor comprising a gate, source and drain, coupled in common source configuration, the width w_G of the gate being optimized to provide noise matching of the transistor,

the first inductor being a source coupled inductor L_E for matching the real part of the input impedance Z_O, and the second inductor being a gate coupled inductor L_B for matching the imaginary part of the input impedance and noise reactance to 0Ω.

5. A structure according to claim 1 comprising a second transistor for input/output buffering, the second transistor coupled to the first transistor in cascode configuration, the size ratio of Q1 to Q2 being determined by the ratio of the peak f_T current density and the minimum noise current density.

6. A structure according to claim 1 wherein the characteristic impedance Z_O is 50Ω.

7. An integrated circuit according to claim 3 wherein the bipolar transistor is selected from the group consisting bipolar junction transistors (BJTs) or heterojunction bipolar transistors (HBTs).

8. An integrated circuit according to claim 7 implemented in silicon.

9. An integrated circuit according to claim 7 implemented in silicon-germanium.

10. An integrated circuit according to claim 7 implemented in a III-V compound semiconductor.

11. An integrated circuit according to claim 7 implemented in GaAs.

12. An integrated circuit according to claim 4 wherein the field effect transistor is selected from the group comprising MOSFETS, MESFETS, JFETS, and HEMT transistors.

13. An integrated circuit according to claim 6 wherein the field effect transistor is a silicon MOSFET.

14. An integrated circuit comprising according to claim 3 comprising second bipolar transistor, coupled in cascode configuration, common base mode, for input/output buffering.

15. A circuit according to claim 14 wherein the size ratio of the emitter lengths of the first and second transistors is determined by the ratio of the peak f_T current density to the minimum noise current density.

16. An integrated circuit comprising according to claim 4 comprising a second field effect transistor, coupled in cascode configuration, common gate mode, for input/output buffering.

17. A circuit according to claim 16 wherein the size ratio of the gate widths of the first and second transistors is determined by the ratio of the peak f_T current density to the minimum noise current density.

18. An integrated circuit including an integrated transistor-inductor structure comprising:

first and second bipolar transistors in cascode configuration, each transistor comprising an emitter, collector and base, the first transistor being coupled in common emitter mode and the second transistor coupled in common base mode, the first transistor having a emitter length I_E, selected to provide the real part of the optimum noise impedance equal to the characteristic impedance of the integrated circuit Z_O, thereby providing noise matching of the transistor at a selected operating frequency;

a first inductor L_E coupled to the emitter of the first transistor, for matching the real part of the input impedance to Z_O, and a second inductor L_B, coupled to the base of the first transistor, for cancelling out the imaginary part of the input impedance and the noise reactance respectively, the circuit thereby providing simultaneous noise and input impedance matching.

19. A circuit according to claim 18 wherein an emitter length l_{E2} of the second transistor is selected to provide that it is biased at the current density at which its cutoff frequency reaches a maximum for maximizing gain and frequency of operation.

20. A circuit according to claim 18 wherein the ratio of the emitter lengths of first and second transistors is determined by the ratio of the peak f_T current density to the minimum noise current density.

21. The circuit according to claim 18 operable as a low noise amplifier, comprising:

means for supplying a first input signal coupled to the first transistor base through the second inductor L_B,

the transistor emitter coupled to an emitter degeneration means comprising the first inductor L_E, and output means coupled to the collector of the first transistor for generating an output signal.

22. The circuit according to claim 18 operable as a mixer circuit, comprising:

means for supplying an first input (RF) signal coupled to the first transistor base through the second inductor L_B,

a second base inductor coupled to the base of the second transistor and means for supplying a second input (LO) signal coupled to the second transistor through the second base inductor;

the transistor emitter coupled to an emitter degeneration means comprising the first inductor L_E, and

output means coupled to the collector of the first transistor for generating an output (IF) signal.

23. An integrated circuit according to claim 21 wherein the output means comprises an LC filter.

24. A silicon integrated circuit structure comprising a integrated transistor-inductor structure for operation as a double balanced mixer, comprising:

an input pair of common emitter transistors Q1 and Q2, a mixing quad comprising two differential pairs of common base transistors Q3 and Q4, and Q5 and Q6, each transistor of the input pair Q1 and Q2 coupled to an emitter of a respective one of the pairs of the mixing quad;

a pair of emitter inductors L_E coupled to the emitters of the input pair Q1 and Q2, the emitter inductors L_E providing emitter degeneration means, and a base inductor L_B coupled to the base of one of first pair of Q1 and Q2, the other base being AC grounded;

input means for supplying differential input (RF) signals coupled to the bases of the input transistor pair through the second inductor LB,

input means for supplying differential second input (LO) signals coupled to respective bases of each pair of transistors of the mixing quad,

output means coupled to collectors of pairs transistors of the mixing quad for generating a differential output IF signal; and

each of the transistors of the input pair Q1 and Q2 having a emitter length I_E, selected to provide the real part of the optimum noise impedance equal to the characteristic impedance of the integrated circuit Z_O, thereby providing noise matching of the transistors at a selected operating frequency;

the emitter inductors L_E coupled to the emitter of the input transistors, for matching the real part of the input impedance to Z_O, and the second inductor L_B, coupled to the base of one of the input transistor, for cancelling out the imaginary part of the input impedance and the noise reactance respectively, the circuit thereby providing simultaneous noise and input impedance matching.

25. An integrated circuit according to claim 24 wherein the size ratio of the transistors in the mixing quad and the input pair is based on ratio of the peak f_T current density and the minimum noise current density.

26. An integrated circuit according to claim 24 including an LO reject filter comprising an series LC filter coupled to between differential IF output ports.

27. An integrated circuit according to claim 25 including a parallel LC resonator tuned on the second RF harmonic as an AC current source coupled in the emitter of the input pair.

28. A silicon integrated circuit structure comprising a transistor-inductor structure for operation as a low noise differential amplifier, comprising:

an input pair of common emitter transistors Q1 and Q2, and an output pair of common base transistors Q3 and Q4 coupled in cascode configuration; a pair of emitter inductors L_E coupled to respective emitters of the input pair Q1 and Q2, and a pair of base inductors L_B coupled to the respective bases of the input pair of Q1 and Q2,

means for receiving a first input signal pairs coupled to respectively to the bases of the first transistor pair through the second inductors L_B,

for generating a pair of output signals at the collectors of the second transistors Q3 and Q4;

each of the transistors of the input pair Q1 and Q2 having a emitter length I_E, selected to provide the real part of the optimum noise impedance equal to the characteristic impedance of the integrated circuit Z_O, thereby providing noise matching of the transistors at a selected operating frequency;

the emitter inductors L_E coupled to the emitter of the input transistors, for matching the real part of the input impedance to Z_O, and the base inductor L_B, coupled to the base of one of the input transistor, for cancelling out the imaginary part of the input impedance and the noise reactance respectively, the circuit thereby providing simultaneous noise and input impedance matching.

29. An integrated circuit according to claim 28 wherein the emitter lengths of the first and second pairs of transistors of the differential amplifier are twice as large as the corresponding emitter lengths in a corresponding single ended amplifier circuit.

* * * * *

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United States Patent [19]

Mitzlaff

[11] Patent Number: 5,307,512

[45] Date of Patent: Apr. 26, 1994

[54] **POWER CONTROL CIRCUITRY FOR ACHIEVING WIDE DYNAMIC RANGE IN A TRANSMITTER**

[75] Inventor: **James E. Mitzlaff**, Arlington Heights, Ill.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **709,459**

[22] Filed: **Jun. 3, 1991**

[51] **Int. Cl.**[5] **H04B 1/04**

[52] **U.S. Cl.** **455/126**; 455/127; 330/144; 330/284

[58] **Field of Search** 455/126, 127, 67.1, 455/102, 115, 118, 52.1; 330/144, 279, 284

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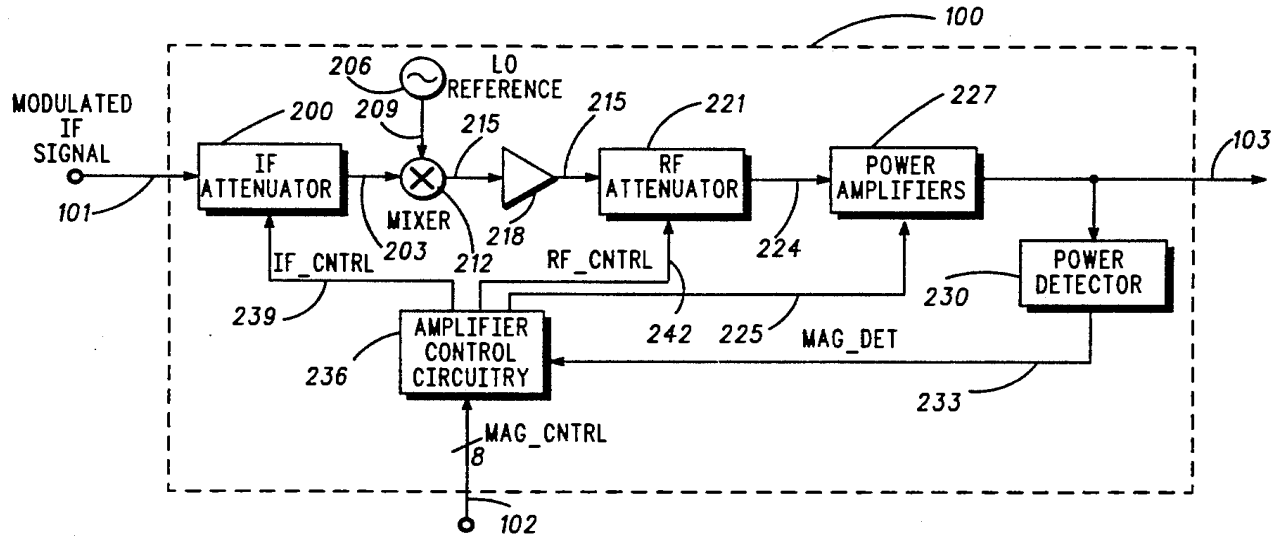
Primary Examiner—Reinhard J. Eisenzopf
Assistant Examiner—Edward Urban
Attorney, Agent, or Firm—Richard A. Sonnentag

[57] **ABSTRACT**

Power control circuitry (**100**) uses two attenuators in the transmit path to achieve wide dynamic range. An intermediate frequency (IF) attenuator (**200**) is placed before a mixer (**212**) in the IF section of the transmit path and a radio frequency (RF) attenuator (**221**) is placed after the mixer (**212**) in the RF section of the transmit path. Power control circuitry (**236**) controls setting of the two attenuators in response to a magnitude control signal (**102**) related to a RF output signal at a desired power level. To conserve battery power of the subscriber unit, only the RF attenuator (**221**) is adjusted when the desired power level is to be within a given range below the maximum transmission level. For ranges below the given range, the RF attenuator (**221**) is set for maximum attenuation and the IF attenuator (**200**) is adjusted.

28 Claims, 2 Drawing Sheets



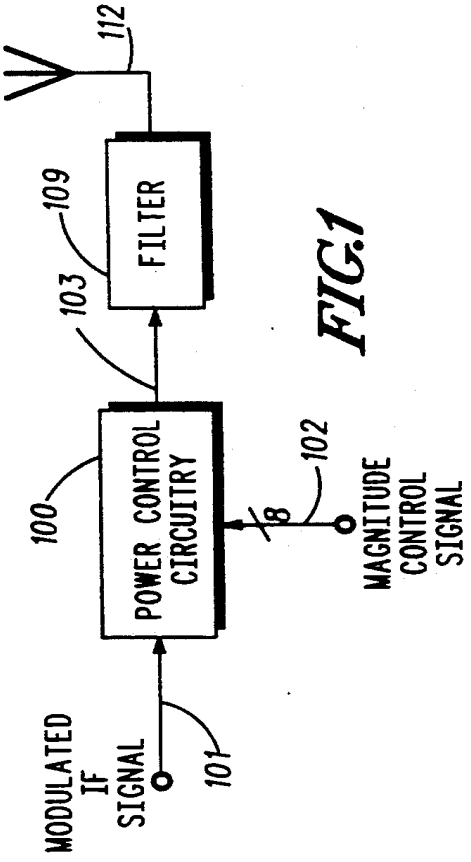

MODULATED IF SIGNAL
101
POWER CONTROL CIRCUITRY
100
103
FILTER
109
112
8
102
MAGNITUDE CONTROL SIGNAL

FIG.1

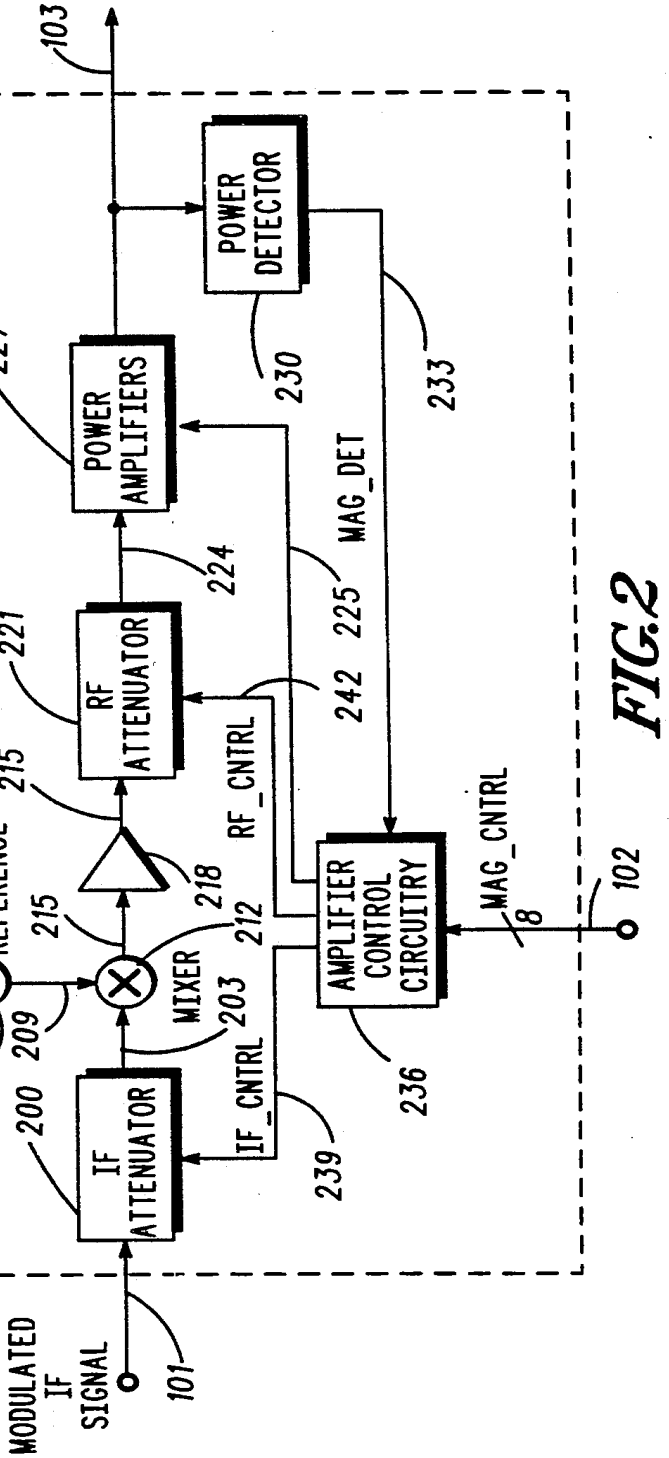

MODULATED IF SIGNAL
101
IF ATTENUATOR
200
IF_CNTRL
239
AMPLIFIER CONTROL CIRCUITRY
236
MAG_CNTRL
8
102
MIXER
203
212
218
LO REFERENCE
206
209
215
RF ATTENUATOR
221
RF_CNTRL
242
POWER AMPLIFIERS
227
224
MAG_DET
225
POWER DETECTOR
230
233
100
103

FIG.2

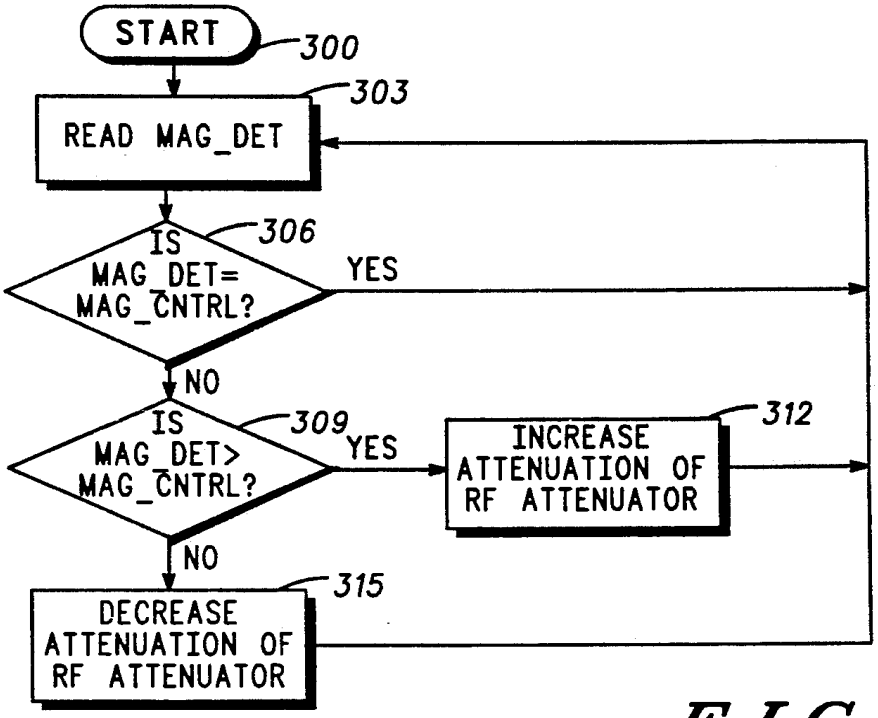

START
300
READ MAG_DET
303
IS MAG_DET= MAG_CNTRL?
306
YES
NO
IS MAG_DET> MAG_CNTRL?
309
YES
INCREASE ATTENUATION OF RF ATTENUATOR
312
NO
DECREASE ATTENUATION OF RF ATTENUATOR
315

FIG. 3

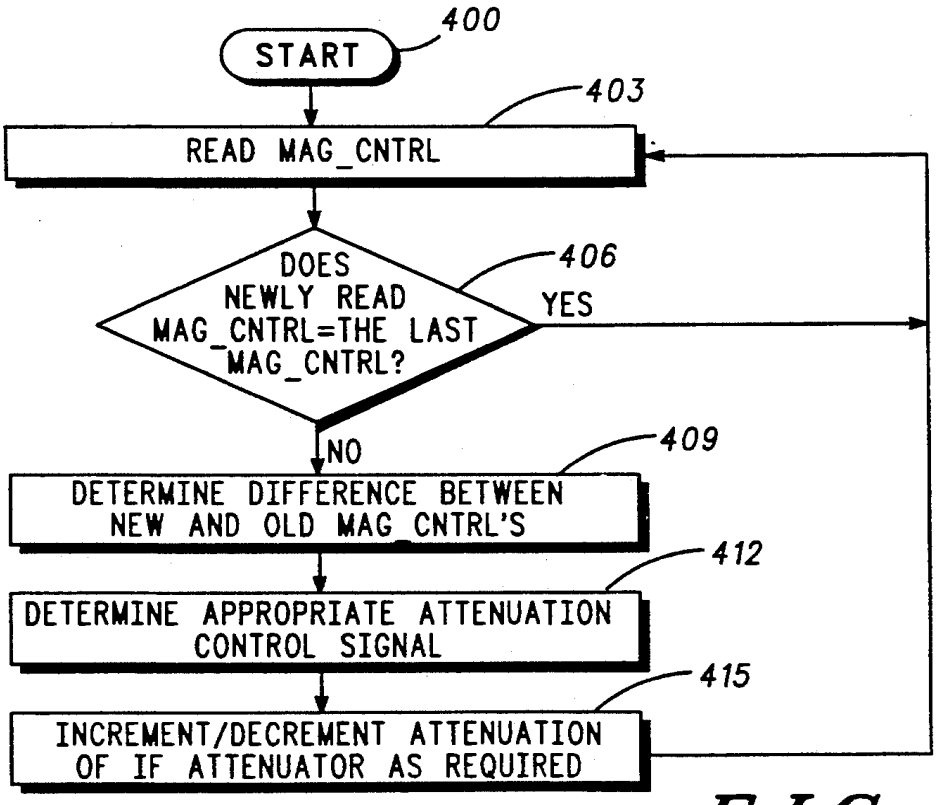

START
400
READ MAG_CNTRL
403
DOES NEWLY READ MAG_CNTRL=THE LAST MAG_CNTRL?
406
YES
NO
DETERMINE DIFFERENCE BETWEEN NEW AND OLD MAG_CNTRL'S
409
DETERMINE APPROPRIATE ATTENUATION CONTROL SIGNAL
412
INCREMENT/DECREMENT ATTENUATION OF IF ATTENUATOR AS REQUIRED
415

FIG. 4

POWER CONTROL CIRCUITRY FOR ACHIEVING WIDE DYNAMIC RANGE IN A TRANSMITTER

FIELD OF THE INVENTION

The present invention is generally related to transmitters in radiotelephones, and more specifically, related to power control circuitry that may be advantageously used in transmitters for radiotelephones.

BACKGROUND OF THE INVENTION

Cellular telephones currently continuously transmit during a telephone call. In a typical scenario, a subscriber unit moves throughout a cell while constantly maintaining communication with a base station located approximately in the center of the cell. As the subscriber unit moves throughout the cell, the received signal strength indication (RSSI) as seen by the base station, varies significantly. This variance has the potential to overload the receiver in the base station when the subscriber unit is very close to the base station.

As personal communication networks (PCN) and code division multiple access (CDMA) type cellular systems evolve, the dynamic range requirements on transmitters becomes more stringent. To avoid overloading of the base station receiver when a subscriber unit is very close to the base station, the subscriber unit must have a typical dynamic range upwards to approximately 80 dB. All current approaches to PA power control, however, are limited to around 40 dB dynamic range because stray RF coupling limits the amount of attenuation that can be achieved to about that level. Stray radiation also becomes a problem when attenuation levels between 40–80 dB are attempted.

Thus, a need exists for power control circuitry which achieves a wide dynamic range while overcoming the problems of stray RF coupling and stray radiation.

SUMMARY OF THE INVENTION

Control circuitry adjusts the level of an output signal. The control circuitry adjusts a priori the level of a signal having a first frequency to produce an adjusted signal having a first frequency, translates the adjusted signal having a first frequency to a translated signal having a second frequency, and adjusts a priori the level of the translated signal having a second frequency to produce the adjusted output signal having a second frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram generally illustrating a RF signal power amplifier employing power control circuitry in accordance with the invention.

FIG. **2** is a block diagram of the power control circuitry in accordance with the invention.

FIG. **3** is a flow chart for the process used by amplifier control circuitry **236** to set RF attenuator **221** in FIG. **2**.

FIG. **4** is a flow chart for the process used by amplifier control circuitry **236** to set IF attenuator **200** in FIG. **2**.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

FIG. **1** illustrates a RF signal power amplifier which may advantageously employ the present invention. A RF signal power amplifier is typically part of a radio transmitter, such as that described in Motorola Instruction Manual No. 68P81039E25, entitled, "Advanced Mobile Phone System", and published by Motorola Service Publications, 1301 E. Algonquin Rd., Schaumburg, Ill. 1979. The RF signal power amplifier in FIG. **1** includes power control circuitry **100** which accepts a modulated IF signal **101**, upconverts the IF signal **101** to a RF output signal **103** and adjusts the IF signal **101** and the RF output signal **103** proportional to a magnitude control signal, MAG_CNTRL **102**. In the preferred embodiment, MAG_CNTRL **102** is an 8-bit digital word used to represent the desired RF output signal at a particular power level. In alternate embodiments, the number of bits in the digital word may vary depending on the number of transmission levels the system requires. Output from the power control circuitry **100** is RF output signal **103** having a desired power level related to the magnitude control signal. The RF output signal is coupled via a filter **109** to an antenna **112**. The output power level developed by the power control circuitry **100** typically amplifies the input signal **101** from approximately one milliwatt to 5 or more watts.

FIG. **2** depicts further detail of the power control circuitry **100** in accordance with the invention. FIG. **2** consists of an IF attenuator **200**, a mixer **212**, a filter and buffer amplifier **218**, a RF attenuator **221**, power amplifiers (PA's) **227**, a power detector **230** and amplifier control circuitry **236**. A modulated IF signal **101** enters IF attenuator **200** and is attenuated by an amount dependent on the value of a first adjustment control signal, IF_CNTRL **239**. In the preferred embodiment, IF attenuator **200** is a balanced mixer type attenuator PAS-3 manufactured by Mini-Circuits and is used to adjust the level of the IF signal **101**. In alternate embodiments, IF attenuator may be realized by employing PIN diode attenuators or gain controllable amplifiers, such as a Hewlett-Packard HPVA-0180 gain controllable amplifier. Output from IF attenuator **200** is an adjusted IF signal **203** which then enters a mixer **212**. The mixer **212** can be any conventional mixer circuit, such as a double balanced, diode type mixer or balanced Gilbert Cell type active mixer to minimize local oscillator (LO) feedthrough and is used to translate the adjusted IF signal **203** to a RF signal **215**. The mixer **212** also has as an input a reference signal **209** which is generated by the LO reference **206**. Output from the mixer **212** is a RF signal **215** which is then filtered and buffered by filter and buffer amplifier **218**. The filter and buffer amplifier **218** are required to remove spurious components from the mixer output and build up the signal to the levels needed to drive subsequent stages. Continuing, the RF signal **215** enters a second attenuator, RF attenuator **221**. In the preferred embodiment, RF attenuator **221** is a balanced mixer type attenuator PAS-2 manufactured by Mini-Circuits and is used to adjust the level of the RF signal **215**. The RF signal **215** is attenuated by an amount depending on the value of a second attenuation control signal, RF_CNTRL **242**. Output from the RF attenuators **221** is an adjusted RF signal **224** which is amplified by power amplifiers **227** to produce the desired RF output signal. The power amplifiers **227** may be any conventional class A, AB, or B power amplifiers which may be driven into saturation for higher efficiency when constant envelope modulation schemes (such as FM) are employed. A power detector **230** detects the magnitude of the desired RF output signal and produces a magnitude detection sig-

nal, MAG_DET 233. The power detector may be any conventional power detector such as diode type detectors or logarithmic amplifier/detector circuitry. Amplifier control circuitry 236 accepts MAG_DET 233, and also MAG_CNTRL 102. Amplifier control circuitry 236 determines IF_CNTRL 239 and RF_CNTRL 242 relative to the difference between MAG_DET 233 and MAG_CNTRL 102.

Amplifier control circuitry 236 is at the heart of the power control circuitry 100 and is unique in that it must control two outputs instead of just one. In the preferred embodiment, a microprocessor, such as a Motorola 68HC11, could be used to digitally control IF attenuator 200 and RF attenuator 221. Digital-to-analog (D/A) converters can be used on each output as required to provide IF_CNTRL 239 and RF_CNTRL 242 in analog form. As digitally controlled attenuators become more commonplace, the D/A converters will not be required. Likewise, in an alternate embodiment, an A/D converter can be used to digitize the output of the power detector 230. In this embodiment MAG_DET 233 would be a digital representation of the desired RF output signal.

Control of IF attenuator 200 and RF attenuator 221 is accomplished as follows. Amplifier control circuitry 236 would allow the desired RF output signal 103 to be within a predetermined power level range or dynamic range, which for purposes of example, might be 80 dB. An adjustment power level range, which is less than the 80 dB dynamic range, is programmed into the microprocessor of amplifier control circuitry 236. This range, again for example purposes, may be anywhere between 0 and 40 dB below the maximum available power level. If the desired RF output signal is to be within this smaller range, only RF attenuator 221 is adjusted. If MAG_CNTRL 102 entering amplifier control circuitry 236 indicates that the subscriber unit must transmit within this 0 to 40 dB range below the maximum, IF attenuator 200 is set for maximum output and a control loop is invoked. FIG. 3 depicts the steps amplifier control circuitry 236 undergoes to set RF attenuator 221 during this process. The process starts at 300 when amplifier control circuitry 236 reads at 303 MAG_DET 233. A test is then performed to determine if MAG_DET 233 is equivalent to MAG_CNTRL 102. If it is, amplifier control circuitry 236 will again read at 303 MAG_DET 233. If MAG_DET 233 is not equivalent to MAG_CNTRL 102, another test is performed at 309 to determine if MAG_DET 233 is greater than MAG_CNTRL 102. If it is, the desired RF output signal 103 is too high and must be attenuated. This is accomplished by amplifier control circuitry 236 by increasing at 312 the amount of attenuation of RF attenuator 221. After the attenuation is increased, amplifier control circuitry 236 will again read at 303 MAG_DET 233. If MAG_DET 233 is not greater than MAG_CNTRL 102, the desired RF output signal 103 is below the level required by MAG_CNTRL 102, and consequently amplifier control circuitry 236 decreases at 315 the attenuation of RF attenuator 221. Again, after the attenuation has been decreased, amplifier control circuitry 236 reads at 303 MAG_DET 233 to determine if the level is as desired.

As long as MAG_CNTRL 102 requests the subscriber to transmit within 40 dB of the maximum (the adjustment power level range), RF attenuator 221 is the only attenuator which is adjusted. This is important for subscriber units which run off of battery power, since less current is used in switching only one of the two available attenuators. Another important reason for controlling RF attenuator 221 at the higher power levels is to minimize power consumed by the PA's 227, which is often directly proportional to PA input/output power. In addition, the current supplied to PA's 227 when higher power levels are required is varied as a function of the required output level. To optimize PA efficiency throughout the adjustment power level range, bias control signal 225 from amplifier control circuitry 236 to the PA's 227 is varied to control PA idle current for Class A and AB PA's. Amplifier control circuitry 236 monitors MAG_CNTRL 102, and when MAG_CNTRL 102 is within the aforementioned adjustment power level range, amplifier control circuitry 236 will set the bias control signal 225 to a predetermined level so as to limit PA current to the minimum level needed to produce the required output power.

When the transmission level is required to be the below the adjustment power level range, amplifier control circuitry 236 will reduce the current supplied to the PA's 227 to a minimum current required to maintain transmission at the required output power level. This output power level, and its corresponding minimum current level, occurs at the bottom of the adjustment power level range. Also at this time, RF attenuator 221 is set to maximum attenuation and IF attenuator 200 is then adjusted to provide for further reductions in RF output power. Use of two attenuators in the transmit path, where the signals attenuated are at different frequencies, allows for the wide dynamic range of the transmitter. The major drawback of single attenuator transmitter paths is that the attenuation is limited to around 40 dB of control range due to stray coupling around the attenuator itself. That is, even though the path through the attenuator can be cutoff completely, some amount of signal always leaks around the attenuator and into succeeding amplifier stages. Two attenuators in the transmit path, where the signals are at different frequencies, avoid the stray coupling problem since the IF signal will not propagate through the RF circuitry, even if there is some IF signal leakage. Attenuating at both IF and RF also minimizes stray radiation, since the level of transmit frequency signal present inside the subscriber unit is greatly reduced.

If the power detector 230 has approximately 80 dB of dynamic range, then a similar feedback loop as that described in FIG. 3 for adjusting IF attenuator 200 through IF_CNTRL 239, could be used for ranges between 40 to 80 dB below the maximum power level. In the preferred embodiment, since detector range is usually limited to below 80 dB, an incremental control scheme using a linear IF attenuator 200 may be incorporated. In the linear IF attenuator 200, the attenuation is "calibrated" so that a given step in IF_CNTRL 239 say 1 V, produces a constant change in power, like 10 dB.

FIG. 4 depicts the steps amplifier control circuitry 236 would undergo to perform the incremental control scheme. The process starts at 400 when amplifier control circuitry 236 reads at 403 MAG_CNTRL 102. A test is then performed at 406 to determine if the newly read MAG_CNTRL 102 is equal to the last magnitude control signal. If it is, IF attenuator 200 does not need to be adjusted and amplifier control circuitry 236 will read at 403 the next MAG_CNTRL 102. If, however, the newly read MAG_CNTRL 102 is not equal to the last MAG_CNTRL 102, amplifier control circuitry 236 will determine at 409 the difference between the new

and the old MAG_CNTRL's. Amplifier control circuitry **236** then determines at **412** the appropriate IF_CNTRL **239** to be applied to IF attenuator **200**. IF attenuator **200** then has its attenuation incremented/decremented at **415** as required. After the attenuation has been incremented/decremented, a new MAG_CNTRL **102** is read at **403** by amplifier control circuitry **236** and the process is repeated.

Thus, needs have been substantially met for power control circuitry which provides wide dynamic range for use in radiotelephone systems where overloading of a base-station receiver must be avoided. The use of an attenuator in the IF branch and an attenuator in the RF branch reduces the affects of stray coupling around the attenuators to effectively increase the dynamic range of the transmitter. This two stage control scheme also provides for improved efficiency by enabling the PA's **227** current to be cut back as the RF output power level is reduced.

What I claim is:

1. Control circuitry for adjusting the level of an output signal comprising:

first means for adjusting a priori the level of a signal having a first frequency to produce an adjusted signal having a first frequency;

means, coupled to said first means for adjusting, for translating said adjusted signal having a first frequency to a translated signal having a second frequency;

second means, coupled to said means for translating, for adjusting a priori the level of said translated signal having a second frequency to produce the adjusted output signal having a second frequency;

means, coupled to said second means for adjusting, for amplifying said adjusted output signal having a second frequency to produce an amplified adjusted output signal having a second frequency;

means, coupled to said means for amplifying, for detecting a magnitude of said amplified adjusted output signal having a second frequency to produce a magnitude detection signal; and

means for controlling said first and second means for adjusting and said means for amplifying based on input from at least said magnitude detection signal and an adjustment control signal.

2. The control circuitry of claim **1** wherein said first means for adjusting further comprises means for attenuating the level of said signal having a first frequency.

3. The control circuitry of claim **1** wherein said first means for adjusting further comprises means for variably amplifying the level of said signal having a first frequency.

4. The control circuitry of claim **1** wherein said second means for adjusting further comprises means for attenuating the level of said translated signal having a second frequency.

5. The control circuitry of claim **1** wherein said second means for adjusting further comprises means for variably amplifying the level of said translated signal having a second frequency.

6. The control circuitry of claim **1** wherein said means for translating further comprises means for generating a reference signal having a third frequency.

7. The control circuitry of claim **6** wherein said means for translating further comprises means for mixing said adjusted signal having a first frequency with said reference signal having a third frequency to produce said translated signal having a second frequency.

8. Power control circuitry for adjusting the power level of a radio frequency (RF) output signal, the power control circuitry having as input an intermediate frequency (IF) signal from a signal source, the power control circuitry comprising:

first means for adjusting a priori the power level of the IF signal to produce an adjusted IF signal;

means, coupled to said first means for adjusting, for translating said adjusted IF signal to the RF output signal;

second means, coupled to said means for translating, for adjusting a priori the power level of said RF output signal to produce an adjusted RF output signal;

means, coupled to said second means for adjusting, for amplifying said adjusted RF output signal to produce an amplified adjusted RF output signal;

means, coupled to said means for amplifying, for detecting a magnitude of said amplified adjusted RF output signal to produce a magnitude detection signal; and

means for controlling said first and second means for adjusting and said means for amplifying based on input from at least said magnitude detection signal and an adjustment control signal.

9. The power control circuitry of claim **8** wherein said means for translating further comprises means for generating a reference signal.

10. The power control circuitry of claim **9** wherein said means for translating further comprises means for mixing said adjusted IF signal with said reference signal to produce said RF output signal.

11. Power control circuitry for adjusting the power level of a radio frequency (RF) output signal over a predetermined power level range in a transmitter, the power control circuitry having as input an intermediate frequency (IF) signal from a signal source, the power control circuitry having the capability to adjust the RF output signal to a desired level and provide at least one adjustment control signal related to the RF output signal at a desired power level, the power control circuitry comprising:

means for providing an adjustment power level range less than or equal to the predetermined power level range;

means for generating a reference signal;

means for detecting a magnitude level of the RF output signal to produce a magnitude detection signal;

means for providing first and second adjustment control signals from the difference between the magnitude detection signal and a magnitude control signal;

first means, responsive to the first adjustment control signal, for adjusting the IF signal when the desired power level of the RF output signal is not within said adjustment power level range;

means, coupled to said first means for adjusting, for mixing said generated reference signal with said adjusted IF signal to produce the RF output signal; and

second means, responsive to the second adjustment control signal, for adjusting said RF output signal when said desired power level of said RF output signal is within said adjustment power level range to produce the RF output signal at the desired power level.

12. The power control circuitry of claim 11 wherein said first means for adjusting further comprises means for attenuating the power level of said IF signal when the desired power level of the RF output signal is not within said adjustment power level range.

13. The power control circuitry of claim 11 wherein said second means for adjusting further comprises means for attenuating the power level of said RF output signal when said desired power level of said RF output signal is within said adjustment power level range.

14. The power control circuitry of claim 11 wherein said second means for adjusting further comprises means for variably amplifying the power level of said RF output signal when said desired power level of said RF output signal is within said adjustment power level range.

15. A method of adjusting the level of an output signal comprising the steps of:

adjusting a priori the level of a signal having a first frequency to produce an adjusted signal having a first frequency;

translating said adjusted signal having a first frequency to a translated signal having a second frequency;

adjusting a priori the level of said translated signal having a second frequency to produce the adjusted output signal having a second frequency;

amplifying said adjusted output signal having a second frequency to produce an amplified adjusted output signal having a second frequency;

detecting a magnitude of said amplified adjusted output signal having a second frequency to produce a magnitude detection signal; and

controlling said steps of adjusting and said step of amplifying based on input from at least said magnitude detection signal and an adjustment control signal.

16. The method of claim 15 wherein said step of adjusting the level of a signal having a first frequency further comprises the step of attenuating the level of said signal having a first frequency.

17. The method of claim 15 wherein said step of adjusting the level of a signal having a first frequency further comprises the step of variably amplifying the level of said signal having a first frequency.

18. The method of claim 15 wherein said step of adjusting the level of said translated signal having a second frequency further comprises the step of attenuating the level of said translated signal having a second frequency.

19. The method of claim 15 wherein said step of adjusting the level of said translated signal having a second frequency further comprises the step of variably amplifying the level of said translated signal having a second frequency.

20. The method of claim 15 wherein said step of translating further comprises the step of generating a reference signal having a third frequency.

21. The method of claim 20 wherein said step of translating further comprises the step of mixing said adjusted signal having a first frequency with said reference signal having a third frequency to produce said translated signal having a second frequency.

22. A method of adjusting the power level of a radio frequency (RF) output signal, the method comprising the steps of:

adjusting a priori the power level of an IF signal to produce an adjusted IF signal;

translating said adjusted IF signal to a RF output signal;

adjusting a priori the power level of said RF output signal to produce an adjusted RF output signal;

amplifying said adjusted RF output signal to produce an amplified adjusted RF output signal;

detecting a magnitude of said amplified adjusted RF output signal to produce a magnitude detection signal; and

controlling said steps of adjusting and said step of amplifying based on input from at least said magnitude detection signal and an adjustment control signal.

23. The method of claim 22 wherein said step of translating further comprises the step of generating a reference signal.

24. The method of claim 23 wherein said step of translating further comprises the step of mixing said adjusted IF signal with said reference signal to produce said RF output signal.

25. A method of adjusting the power level of a radio frequency (RF) output signal over a predetermined power level range in a transmitter incorporating power control circuitry, the power control circuitry having as input an intermediate frequency (IF) signal from a signal source, the power control circuitry having the capability to adjust the RF output signal to a desired level and provide at least one adjustment control signal related to the RF output signal at a desired power level, the method comprising the steps of:

providing an adjustment power level range less than or equal to the predetermined power level range;

generating a reference signal;

detecting a magnitude level of the RF output signal to produce a magnitude detection signal;

providing first and second adjustment control signals from the difference between the magnitude detection signal and a magnitude control signal;

adjusting, based on the first adjustment control signal, the IF signal when the desired power level of the RF output signal is not within said adjustment power level range;

mixing said generated reference signal with said adjusted IF signal to produce the RF output signal; and

adjusting, based on the second adjustment control signal, said RF output signal when said desired power level of said RF output signal is within said adjustment power level range to produce the RF output signal at the desired power level.

26. The method of claim 25 wherein said step of adjusting the IF signal further comprises the step of attenuating the power level of said IF signal when the desired power level of the RF output signal is not within said adjustment power level range.

27. The method of claim 25 wherein said step of adjusting said RF output signal further comprises the step of attenuating the power level of said RF output signal when said desired power level of said RF output signal is within said adjustment power level range.

28. The method of claim 25 further comprising the steps of:

amplifying said RF output signal at a desired level; and

varying a current supplied at said step of amplifying when the desired power level of the RF output signal is within said adjustment power level range.

* * * * *

Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer

P. J. Sullivan, B. A. Xavier, and W. H. Ku

Abstract—**This paper demonstrates the low voltage operation of a doubly balanced Gilbert mixer fabricated in a 0.8-μm CMOS process and operating as both a down-converter and an up-converter. As a down-converter with an RF input of 1.9 GHz, the mixer has a single sideband noise figure as low as 7.8 dB and achieved down-conversion gain for supply voltages as low as 1.8 V. As an up-converter, the mixer demonstrates 10 dB of conversion gain at an RF frequency of 2.4 GHz with an applied local oscillator (LO) power of −7 dBm and LO-RF/LO-IF isolation of at least 30 dB. Up-conversion gain was achieved over a 5-GHz bandwidth and at supply voltages as low as 1.5 V. The mixer presented demonstrates the lowest single side band noise figure for a CMOS doubly balanced down-converting mixer and the highest frequency of operation for a mixer fabricated in CMOS technology to date.**

Index Terms— **CMOS integrated circuits, frequency conversion, microwave measurement, microwave mixer, mixer noise, mixers, power demand, scattering parameters measurement.**

I. Introduction

A CMOS RF up/down converter would allow a considerable increase in transceiver integration and a reduction in transceiver cost. A low supply voltage is desired for hand-held wireless applications to reduce the weight from the number of stacked battery cells and for the corresponding reduction in power dissipation in the digital circuitry. Mixers are an especially important building block in transceiver design, because the receiver dynamic range is often limited by the first down-conversion mixer. The design of mixers forces many compromises between conversion gain, local oscillator (LO) power, linearity, noise figure, port-to-port isolation, voltage supply, and current consumption. The most fundamental choice in FET mixer design is whether to use an active or a passive mixer. Active FET mixers achieve conversion gain and require lower LO power than their passive counterparts. Passive FET mixers (operating FET's in the linear region) are a well-known mixing technique; they typically demonstrate conversion loss and excellent intermodulation performance at the expense of LO power [1], [2]. A reduced LO drive is a significant advantage in low-voltage/low-power IC design because large LO drives are difficult to generate in a low-voltage environment and result in an increase in power dissipation. This also dictates increased LO-RF/LO-IF isolation in order to maintain the same rejection as would be obtained with a lower LO drive. The primary advantage of a passive mixer is increased dynamic range at the expense of LO drive. As transceiver integration is increased and passive off-chip filters are eliminated, extensive on-chip LO-RF/LO-IF isolation will be required to compensate for the reduced performance of on-chip filtering. Doubly balanced mixers have inherent port-to-port isolation making the doubly balanced structure ideal for integrated circuit design. The doubly balanced bipolar Gilbert cell mixer is favored in integrated circuit applications. A typical Gilbert cell mixer has a stack of three transistors and a load resistor between the voltage rails. As the voltage supply is reduced, it is important to maintain dynamic range for transceiver performance. This paper investigates the low voltage performance of a CMOS Gilbert mixer to demonstrate CMOS as a potential RF technology.

Recent publications in the area of RF CMOS mixers have focused on down-conversion applications. Passive CMOS mixers operated in the linear region [3], [4] have shown excellent input third-order intercept points (IIP3) but poor conversion gain, poor noise figure, and, demand LO drives of greater than +10 dBm. An active doubly balanced mixer with cascoded N- and P-channel devices in a Gilbert topology [5] takes advantage of excellent current reuse, however, the use of P-channel devices in the RF stage limits the frequency of operation. A doubly balanced Gilbert cell mixer design for a zero IF receiver [6] uses P-channel devices as current sources for the IF load. P-channel current sources are unsuitable in a traditional heterodyne architecture with a high intermediate frequency, because the poor transconductance (g_m) of P-channel devices results in physically large P-channel devices. These devices have large shunt capacitance that attenuate high IF signals. Active mixers with resistive loads enable a high IF frequency for down-conversion [7] and make excellent up-converters. Recent publications [8], [9] describe passive CMOS mixers configured as up-converters. These circuits have displayed conversion loss and require a large LO drive. The doubly balanced Gilbert cell mixer described employs an all N-channel topology for high frequency operation. The mixer is suitable for both up-conversion and down-conversion, yet requires only a modest LO drive (−7 dBm) requirement to achieve conversion gain, excellent noise performance and LO-RF/LO-IF isolation.

II. Gilbert Mixer

A doubly balanced CMOS mixer was designed based on a Gilbert cell topology [10], Fig. 1. The mixer has conversion gain and requires a reduced LO power when compared with passive designs. Source degeneration in the tail of the differential amplifier section was not applied. Thus, the mixer configuration was optimized for conversion gain and noise figure rather than linearity or IIP3. To maximize the fre-

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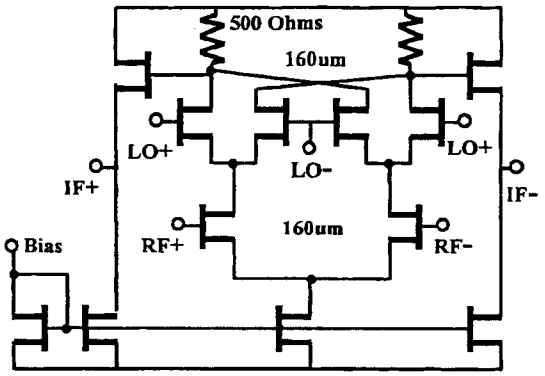

Fig. 1. Schematic.

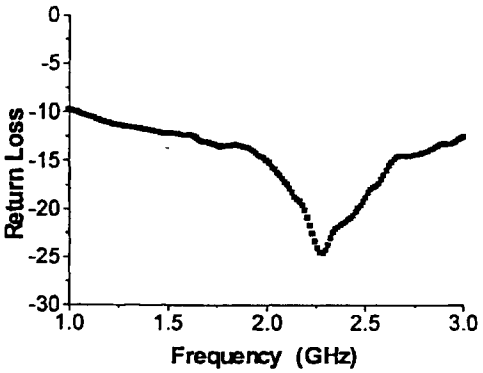

Fig. 2. Output match $|S_{22}|$ for the up-converter with 7.1 mA in the source follower output buffer.

quency of operation for up-conversion, resistive loading of the mixer was chosen. A resistive load has the added benefit of presenting a broad-band match for the up-converter at the mixer's RF output port. The RF and LO ports were biased from off-chip voltage sources through 10-KΩ resistors. The current consumption of the mixer was controlled by current mirrors that regulated current to the Gilbert cell mixer and to an output buffer. The output buffer was a common source amplifier which provided wideband on-chip impedance matching. The circuit requires no inductors on or off chip and buffers the 500-Ω (polysilicon) mixer load from the 50-Ω impedance of the measuring device. The entire mixer had an active area of less than 300 $\times$ 300 μm^2. The CMOS process was a two-layer metal process with a minimum gate length (drawn) of 0.8 μm, effective gate length (L_{eff}) of 0.45 μm. The gate-source threshold voltage for the NMOS devices was 0.7 V (with 0 V body bias) and no special channel implants were used to lower the threshold voltage. A salicide process and the physical layout of multiple gate fingers aided in the reduction of gate resistance, which improved the MOSFET's high-frequency performance. To evaluate the high-frequency performance of the CMOS process, on-wafer small signal scattering (S) parameter measurements were made. Test structures in a common source-substrate configuration were fabricated in the CMOS process for measurement with ground-signal-ground coplanar probes. For the 0.8-μm drawn (0.45-μm L_{eff}) NMOS device, the unity-current-gain cutoff frequency (f_t) was extrapolated to be 16 GHz, and the unity-power-gain cutoff frequency ($f_{\max}$) was measured to be 28 GHz. All measurement conditions were taken with 2-V drain-to-source and 2-V gate-to-source bias. The measured f_t and $f_{\max}$ are similar to other published results for NMOS devices in a standard 0.5-μm salicided CMOS process [11].

The mixer was placed inside a plastic surface mount package (SSOP) which was soldered onto a standard fiber glass printed circuit board (FR4). Careful attention was given to printed circuit board (PCB) layout and package pinout selection to maintain LO-RF/LO-IF isolation. 50-Ω microstrip lines mated the narrow pitch package pins to SMA connectors. The RF, IF, and LO signals were fed on/off the chip differentially into passive 180° -3 dB hybrids.

For testing purposes only, all the mixers ports (RF, LO, and IF) where matched to 50 Ω to conduct proper radio frequency power measurements. Operating as a down-conversion mixer, the measured input impedance at the RF input port was primarily capacitive in nature due to the CMOS gate. From $|S_{11}|$ measurements, it was estimated that a 10.5-nH series inductance was required for a narrow-band reactive input match at the RF ports. The packaging parasitic of the plastic SSOP package, lead frame, and bond wire provided an estimated 3.5-nH series inductance. An additional 7 nH of series inductance was needed and could be implemented as either a lumped element or distributed element matching network. A transmission line segment less than 1/4 wavelength long can approximate capacitance or inductance and may be used to match reactive components. These distributed element matching networks are commonly implemented in monolithic microwave integrated circuits (MMIC's) because 1/4 wavelength structures are physically realizable structures on-chip at X-band frequencies (8–12 GHz) and above. At RF frequencies, 1/4 wavelength structures are not physically realizable on chip but are realizable on a PCB board. A convenient matching technique at RF frequencies is stub tuning. This is implemented as a shunt capacitor sliding along the PCB microstrip transmission feed line. At the RF frequencies of 1.9 GHz and with the additional amount of series inductance required (7 nH), the match was implemented as a stub-tuned distributed element match. This resulted in a more economical and higher Q matching network than would have been possible with a lumped element series inductance match using commercially available surface mount inductors. The resulting match was narrow-band with $|S_{11}|$ better than -8 dB for the RF ports. For the case of the up-conversion mixer, output RF matching was accomplished by varying the bias current of the source follower buffer stage which sets the transconductance (g_m) of the buffer stage to $1/g_m = 50\ \Omega$. Applying this technique allowed the up-conversion mixer/buffer to achieve a broad-band output impedance match $|S_{22}|$ of better than -10 dB over a 2-GHz bandwidth with a drain current of 7.1 mA in the buffer, Fig. 2.

The LO was fed into a passive hybrid as a sine wave with a typical input power of -7 dBm single ended. After passing through the passive hybrids, the LO entered the cross coupled mixer core as a differential input with each side at -10 dBm input power. Each side of the LO input was stub-tune-matched

on the PCB to a 50 Ω system resulting in $|S_{11}|$ better than −7 dB for the LO ports. The −10 dBm of LO power driven into each side of the mixing core through the matching network is a large enough LO power to quickly switch the FET's from their saturated region to their cutoff region and vice versa, because the mixer core FET's are biased near ($V_{gs} = V_t$) threshold. The advantage in biasing the mixer core FET's near threshold are: it allows a reduced LO power to drive the FET's like ideal switches, it also allows the mixer to operate with very low supply voltage with the disadvantage of slightly increasing distortion. The low voltage operation comes about because the transistors are being operated with small $V_{gs} - V_t$ and the transistors stay in the saturation region for very low supply voltages. With a 3-V supply, the $V_{ds\,sat}$ of the mixer core transistors is exceeded by nearly 1 V. As voltage supply is decreased the major effect is a reduction of V_{ds}, and the mixer core transistors continue to operate in the saturation region until $V_{ds} < V_{gs} - V_t$, when the transistor enters the linear region. Once the transistors fall out of saturation the conversion gain falls off dramatically.

III. Measurements

The measured LO and signal powers have been corrected to compensate for the insertion loss of the passive hybrids. No other correcting factors, such as board loss have been included in the measurements. Thus, the conversion gain reported is the power gain of the Gilbert mixer and buffer combination together measured into a 50-Ω system at both the input and output. The single sideband noise figure measurement (SSB NF) was further corrected to compensate for the insertion loss of the narrow-band RF filter and was measured with a standard noise figure meter. The mixer was measured in both up-converting and down-converting modes.

A. Measured Down-Converter Performance

The down-converter was tested over a variety of supply voltages with an RF frequency of 1.9 GHz, LO frequency of 1.65 GHz, and an IF frequency of 250 MHz. At a particular supply voltage, conversion gain and SSB NF were optimized by adjusting four variables: LO input power, total current, and the dc bias points of the LO and RF ports. Once optimum noise figure and conversion gain were attained, two-tone IP3 measurements, single-tone −1 dB compression, conversion gain, and SSB NF measurements were taken. The down-conversion mixer performance over supply voltage was compiled into tabular form and is displayed in Table I. The table displays the total measured current of the mixer and buffer combined. The measured dc current tracked well with simulations, thus, the current consumption can be further subdivided into mixer and buffer contributions.

At a supply voltage of 2.7 V, conversion gain and SSB NF versus LO input power are displayed in Fig. 3. Three regions of mixer operation as a function of LO power can be inferred from Fig. 3. The first region is the low LO power region, where a dB increase in LO power results in a dB improvement in conversion gain; similarly, a dB increase in LO power causes a dB reduction in the SSB NF. The second region is the optimal

TABLE I
DOWN-CONVERTER PERFORMANCE AT RF = 1.9 GHz, IF = 250 MHz

Supply Voltage	V	1.8	2.1	2.3	2.5	2.7	3.0	4.0	5.0
LO Power (1.65 GHz)	dBm	-8	-8	-8	-8	-8	-8	-5	-3
SSB NF (50Ω)	dB	10.2	9.4	9.0	9.0	8.8	8.5	8.2	7.8
Conversion Gain	dB	.5	2.4	3.7	4.7	5.5	6.5	8.7	9.7
Input IP3	dBm	-6	-5.5	-5	-4	-3.5	-3	-1.5	-1
Input -1 dB Compression	dBm	-15	-14.5	-14	-13.5	-13	-12	-10	-9
Current used in Mixer	mA	2.2	2.4	2.7	3.1	3.3	3.5	4.4	5.9
Current used in Buffer	mA	2.6	3.4	4.2	6.1	7.7	9.6	16.1	20.7
Total Current	mA	4.8	5.8	6.9	9.2	11	13.1	20.5	26.6

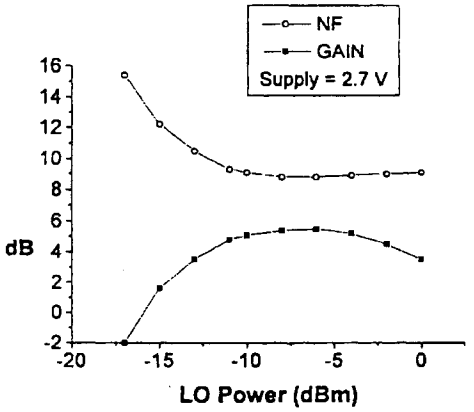

Fig. 3. Down-conversion gain and noise figure as a function of LO power.

LO power region where both the conversion gain and noise figure are constant for a broad region of LO power. A third region of operation exists where the LO power is overdriving the mixer. This results in a reduction in conversion gain due to the subtracting nature of the third-order harmonic. A plot of conversion gain and SSB NF as a function of supply current at a supply voltage of 2.7 V is given in Fig. 4. The general trend of maximum conversion gain occurring at minimum noise figure held for all supply voltages measured. The noise figure had a broad minimum as a function of supply current while the conversion gain was dependent on the supply current. The optimum measured conversion gain is 5.5 dB with an associated minimum SSB NF of 8.8 dB at a supply voltage of 2.7 V, the data is recorded in Table I.

Summarizing Table I: At a 5-V supply, the mixer had a conversion gain of 9.7 dB, an SSB NF of 7.8 dB, and an IIP3 of −1 dBm. With a supply voltage of 1.8 V, the mixer had a conversion gain of 0.5 dB, with an LO drive of −8 dBm, an SSB NF of 10.2 dB, and an IIP3 of −6 dBm, while dissipating 4.0 mW in the Gilbert cell and 4.7 mW in the output buffer. As the supply voltage and power is increased, noise figure and IIP3 improve, resulting in higher dynamic range for the mixer. The SSB NF of 7.8 dB is the lowest published value for this type of mixer. Furthermore, it is interesting to note that in a Gilbert cell mixer, the conversion gain, IIP3, and noise figure are linked. The measured downconversion performance of the mixer presented has a similar distribution of conversion gain, IIP3, and noise figure as a previously measured undegenerated CMOS Gilbert cell downconversion mixer [12].

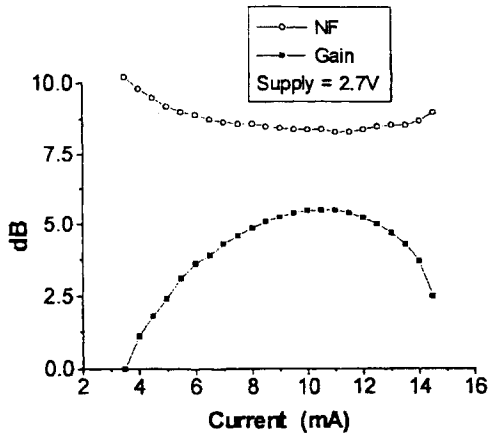

Fig. 4. Down-conversion gain and noise figure as a function of current.

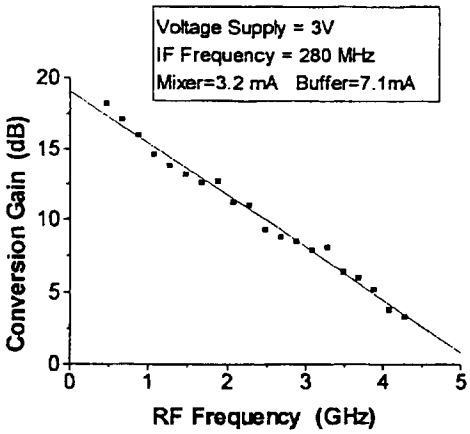

Fig. 5. Up-conversion gain as a function of frequency.

TABLE II
DOWN-CONVERSION PERFORMANCE FOR MATCHED AND UNMATCHED CASES. RF FREQUENCY = 1.9 GHz, IF FREQUENCY = 250 MHz, 2.7 V

		Matched	Unmatched
LO Power (1.65 GHz)	dBm	-8	-4
SSB NF (50Ω)	dB	8.8	13.6
Conversion Gain	dB	5.5	0.5
Input IP3	dBm	-3.5	+1.5
Input -1 dB Compression	dBm	-13	-8

To investigate down-converter performance without distributed matching networks, the shunt capacitors were first taken off the LO inputs. The matched LO port had an $|S_{11}|$ better than -9 dB. With no LO matching network $|S_{11}|$ was broadband with $|S_{11}|$ about -2.1 dB. Removal of all LO matching caused the conversion gain, SSB NF, and output-referred third-order intercept point (OIP3) to decrease by 1 dB, meaning that the IIP3 remained the same. If the LO power was then increased by 4–5 dB, both the conversion gain and the noise figure recovered and similar performance to the LO matched case could be attained. The RF input match $|S_{11}|$ at the RF frequency was narrow-band matched with $|S_{11}|$ better than -10 dB. With no RF matching network, $|S_{11}|$ was -2.3 dB. Taking off all RF matching caused the conversion gain to decrease by 5 dB and the SSB NF decreased by 4.8 dB. The OIP3 stayed the same, implying that the IIP3 improved by 5 dB. Overall optimized performance for the downconversion mixer in the unmatched case is compared to the matched case under the same bias conditions in Table II.

B. Measured Up-Converter Performance

To demonstrate the high frequency performance and wide bandwidth of the CMOS up-converter, conversion gain was measured while both the RF and LO signals were simultaneously swept to give up-conversion gain as a function of RF output frequency with a fixed IF input frequency, Fig. 5. The output spectrum was double sideband with the carrier suppressed. The lower sideband had generally a few more dB of conversion gain than the upper side band (USB). Fig. 5 shows an up-conversion gain of 17 dB at an RF output frequency of 900 MHz and at an RF output frequency of 2.4 GHz, the up-conversion gain is 12 dB. The up-conversion gain as a function of RF frequency followed a slope of -20 dB/decade characteristic of a single pole system. The unity gain crossover frequency of the mixer was 5 GHz.

The LO-RF isolation of an up-converter is especially important since, in general, the LO frequency is close to the desired RF signal frequency and is thus difficult to filter. Due to intermodulation requirements, the LO power is typically an order of magnitude larger than the IF input, thereby compounding the problem. For LO frequencies below 3 GHz the doubly balanced up-converter has LO-RF/LO-IF isolation in excess of 30 dB with as much as 40 dB at certain frequencies. For LO frequencies in the 3–5 GHz range the LO-RF/LO-IF isolation was better than 25 dB.

The OIP3 was measured by applying a two-tone test while sweeping the LO frequency and maintaining a constant IF input frequency of 280 MHz, Fig. 6. The decrease in OIP3 as a function of frequency seems to follow the gain dependence on frequency, Fig. 5. Thus, faster devices (shorter gate length CMOS process) could improve the gain and linearity of the up-conversion mixer. The output -1 dB compression point was measured at an RF output frequency of 2.4 GHz and was -13 dBm, which is 9 dB less than the OIP3. This 9 dB difference between output -1 dB compression point and output IP3 generally held over all frequencies and compares well with the predicted 10 dB difference between OIP3 and -1 dB gain compression point.

To examine the mixer's LO power requirement, conversion gain was measured at an RF output frequency of 2.4 GHz while sweeping LO power. A peak conversion gain of 12 dB was achieved with +3 dBm LO power. Reducing LO power to -7 dBm resulted in a modest reduction of conversion gain to 10 dB, Fig. 7.

The low voltage capability of the CMOS up-conversion mixer was demonstrated by measuring conversion gain (RF = 2.4 GHz) while sweeping the supply voltage, Fig. 8. Up-conversion gain is achieved for supply voltages as low as 1.5 V. The up-converting mixer performance at an RF output frequency of 2.4 GHz is summarized in Table III.

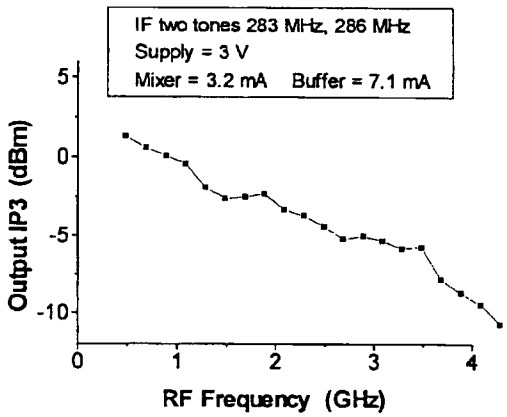

Fig. 6. Two-tone test for output third-order intercept point as a function of up-conversion output frequency.

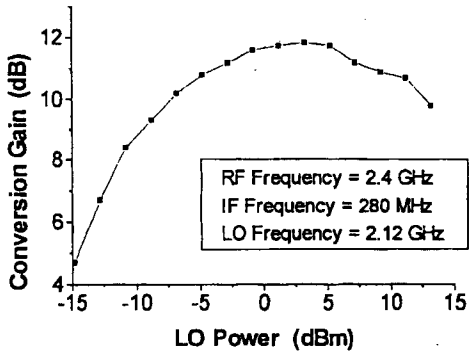

Fig. 7. Up-conversion gain as a function of LO power.

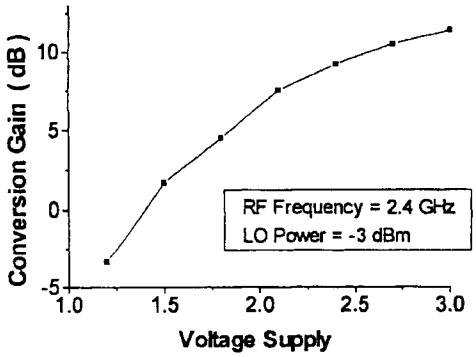

Fig. 8. Up-conversion gain as a function of voltage supply.

From Fig. 5, the upconverter demonstrates conversion gain to 5 GHz. This is the highest RF output frequency generated by an upconverting mixer realized in a standard CMOS technology.

IV. Conclusion

The Gilbert cell mixer demonstrates excellent performance as both an up-converter and a down-converter. The Gilbert down-conversion mixer performance at an RF input frequency of 1.9 GHz is summarized in Table I. The mixer demonstrates down-conversion gain for supply voltages as low as 1.8 V. The up-converter demonstrates up-conversion gain for supply voltages as low as 1.5 V and up-conversion conversion gain for frequencies as high as 5 GHz with wideband on-chip matching requiring no inductors. The up-converting mixer achieves the highest published RF output frequency with a positive conversion gain for a CMOS upconverting mixer. The down-converting mixer achieves the lowest published noise figure for this class of mixer, 7.8 dB SSB. The reduced LO power requirement and low voltage operation make the Gilbert cell mixer look attractive for down-converter and up-converter applications in an all-CMOS transceiver. Though it should be noted that the performance of a CMOS Gilbert cell mixer implemented in a complete CMOS RFIC transceiver is expected to be lower than the measured performance of this mixer because of the inability to generate ideal fully differential RF and LO signals on chip and poorer on-chip matching.

TABLE III
Up-Conversion Mixer Performance at 2.4 GHz

RF Frequency	2.4 GHz
LO frequency	2.12 GHz
IF Frequency	280 MHz
Input LO Power (single ended)	-7 dBm
Conversion Gain (power)	10 dB
Output -1 dB Compression Point	-13 dBm
Output Third Order Intercept	-4 dBm
Voltage Supply	3 V
Total Current	10.3 mA
Current in Mixer	3.2 mA
Current in Buffer	7.1 mA
LO-RF / LO-IF feed-through	< -30 dB

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